LAB MANUAL

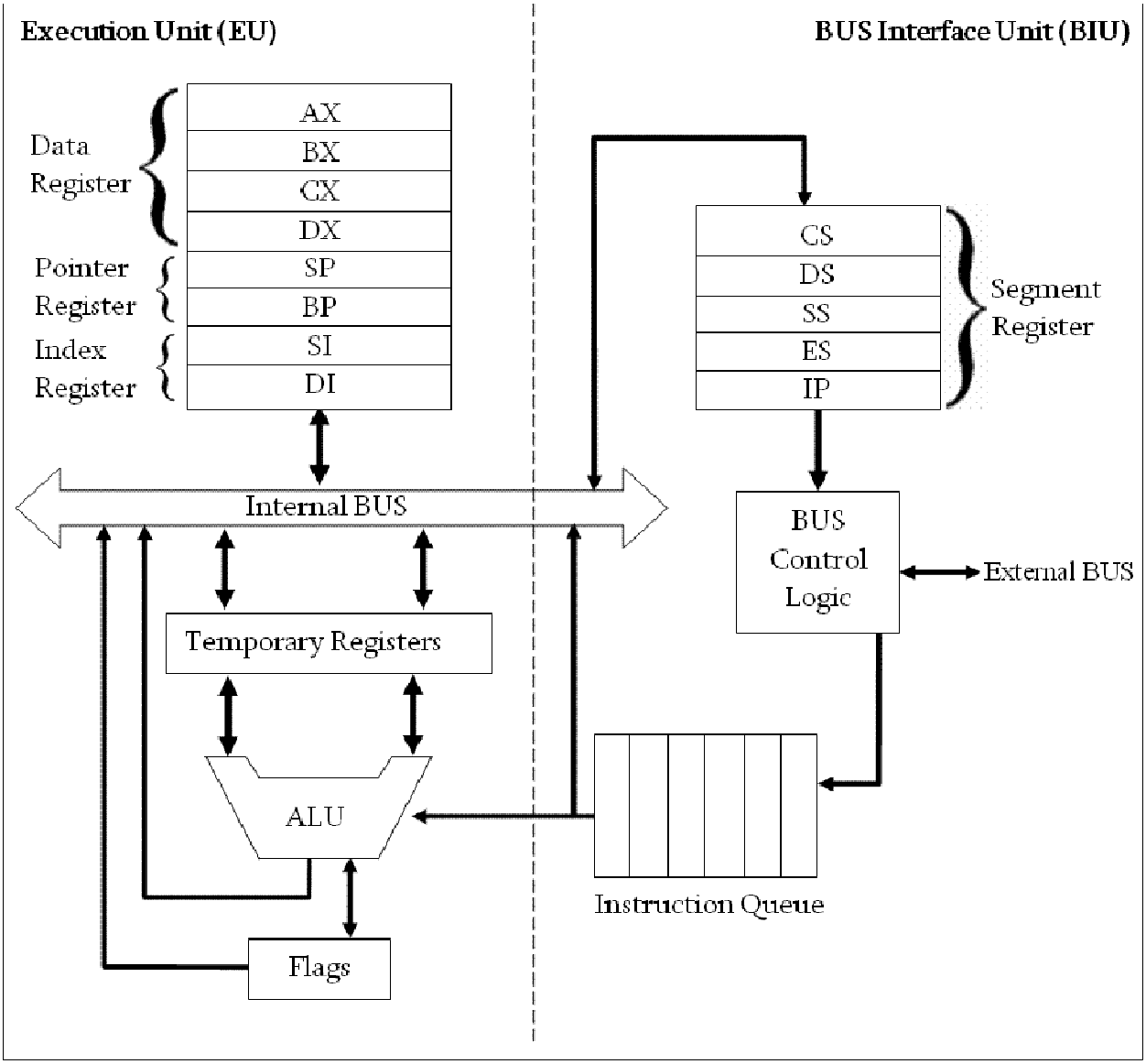
MICROPROCESSOR LAB

SEMESTER 4: COMPUTER ENGINEERING

EXPERIMENT:1

AIM: To familiarize with 8086 Microprocessor

DESCRIPTION:



The **8086** is a 16-bit microprocessor chip designed by Intel between early 1976 and mid-1978, when it was released. The Intel 8088, released in 1979, was a slightly modified chip with an external 8-bit data bus (allowing the use of cheaper and fewer supporting logic chips), and is notable as the processor used in the original IBM PC.

The 8086 gave rise to the x86 architecture which eventually turned out as Intel's most successful line of processors. All internal registers, as well as internal and external data buses, are 16 bits wide, firmly establishing the "16-bit microprocessor" identity of the 8086. A 20-bit external address bus gave a 1 MB physical address space (2^{20} = 1,048,576). This address space was addressed by means of internal 'segmentation'. The data bus was multiplexed with the address bus in order to fit a standard 40-pin dual in-line package. 16-bit I/O addresses meant 64 KBof separate I/O space (2^{16} = 65,536). The maximum **linear** address space was limited to 64 KB, simply because internal registers were only 16 bits wide. Programming over 64 KB boundaries involved adjusting segment registers (see below) and remained so until the 80386 introduced wider (32 bits) registers (and more advanced memory management hardware).

Micro architecture of 8086 microprocessor

The Micro architecture of a processor is its internal architecture that is the circuit building blocks that implement the software and hardware architecture of the 8086 micro processor.

The micro architecture of a 8086 employ parallel processing, that is they are implemented with several simultaneously operating processing units. They have dedicated functions and they operate at the same time. This results in efficient use of the system bus and higher performance for the 8086 processor. The micro architecture of 8086 is classified into two parts: 1) Bus Interface Unit 2) Execution Unit. The BIU provides H/W functions, including generation of the memory and I/O addresses for the transfer of data between the outside world -outside the CPU. The EU receives program instruction codes and data from the BIU, executes these instructions, and store the results in the general registers. By passing the data back to the BIU, data can also be stored in a memory location or written to an output device. Note that the EU has no connection to the system buses. It receives and outputs all its data thru the BIU.

Bus Interface Unit (BIU)

This unit handles all transfer of data and addresses on the buses for the EU(execution unit). This unit sends out addresses, fetches instructions from memory, reads data from ports and memory and writes data to ports and memory.

Different Parts of BIU:
a.Segment Register
b.Instruction Pointer
c.The Queue

1.)Segment Register:- BIU contains four 16-bit segment registers as follows:

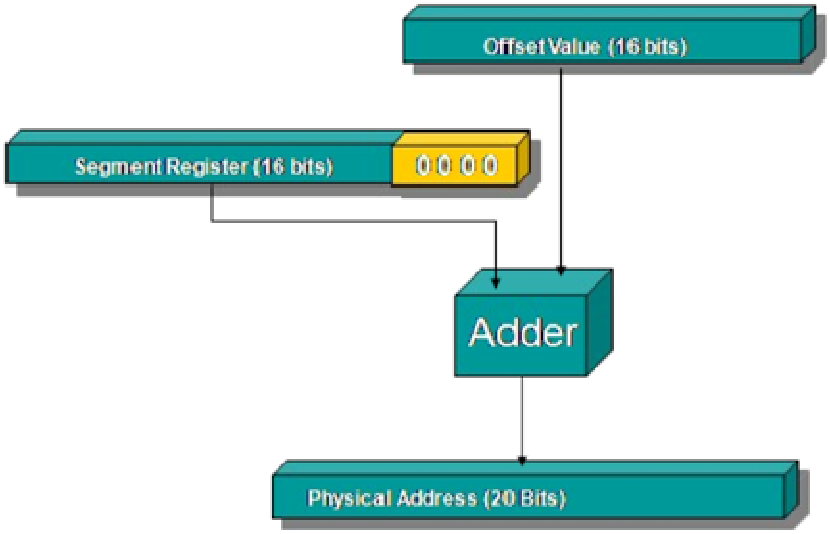
Code segment (CS) register
Stack segment (SS) register
Extra segment (ES) register
Data segment (DS) register

Function of Segment Register:-

Ø In 8086 complete 1MB memory is divided into 16 logical segments.
Ø Each segment thus contains 64 KB of memory.
Ø While addressing any location in the memory bank, the Physical address is calculated from two parts, the first part is Segment address, and the second is Offset.
Ø The segment registers contain 16-bit segment base addresses related to different segments.
Ø Thus the CS, DS, ES, SS segment registers, respectively contain the segment addresses for the Code, Data, Extra and Stack segments.
Ø They may or may not be physical separated.
Ø Each segment register contains a 16-bit base address that points to the lowest-addressed byte of that particular segment in memory.

Memory Address Generation

- The BIU has a dedicated adder for determining physical memory addresses



Generation of physical address:-

Segment address- 1005H
Offset address - 5555H
Segment address-1005H- 0001 0000 0000 0101
Shifted by 4-bit positions-0001 0000 0000 0101 0000
+
Offset address - 0101 0101 0101 0101
Physical address -0001 0101 0101 1010 0101
1 5 5 A 5

Instruction Pointer:-

- It is 16-bit register, which identifies the location of the next word of instruction code that is to be fetched in the current code segment.
- IP contains an offset instead of the actual address of the next instruction.
- The 20-bit address produced after addition of the offset stored in IP to segment base address in the CS is called the Physical address of the code byte.

The Queue:-

- The last section of BIU is the FIFO group of registers called a queue. It is basically a group of registers.
- This arrangement makes possible for the BIU to fetch the instruction byte while EU is decoding an instruction or executing an instruction which does not require use of buses.
- This arrangement is called pipelining.
- This is done to speed up the program execution.

Registers

Most of the registers contain data/instruction offsets within 64 KB memory segment. There are four different 64 KB segments for instructions, stack, data and extra data. To specify where in 1 MB of processor memory these 4 segments are located the 8086 microprocessor uses four segment registers:

Code segment (CS) is a 16-bit register containing address of 64 KB segment with processor instructions. The processor uses CS segment for all accesses to instructions referenced by instruction pointer (IP) register. CS register cannot be changed directly. The CS register is automatically updated during far jump, far call and far return instructions.

Stack segment (SS) is a 16-bit register containing address of 64KB segment with program stack. By default, the processor assumes that all data referenced by the stack pointer (SP) and base pointer (BP) registers is located in the stack segment. SS register can be changed directly using POP instruction.

Data segment (DS) is a 16-bit register containing address of 64KB segment with program data. By default, the processor assumes that all data referenced by general registers (AX, BX, CX, DX) and index register (SI, DI) is located in the data segment. DS register can be changed directly using POP and LDS instructions.

Extra segment (ES) is a 16-bit register containing address of 64KB segment, usually with program data. By default, the processor assumes that the DI register references the ES segment in string manipulation instructions. ES register can be changed directly using POP and LES instructions.

It is possible to change default segments used by general and index registers by prefixing instructions with a CS, SS, DS or ES prefix.

All general registers of the 8086 microprocessor can be used for arithmetic and logic operations. The general registers are:

Accumulator register consists of 2 8-bit registers AL and AH, which can be combined together and used as a 16-bit register AX. AL in this case contains the low-order byte of the word, and AH contains the high-order byte. Accumulator can be used for I/O operations and string manipulation.

Base register consists of 2 8-bit registers BL and BH, which can be combined together and used as a 16-bit register BX. BL in this case contains the low-order byte of the word, and BH contains the high-order byte. BX register usually contains a data pointer used for based, based indexed or register indirect addressing.

Count register consists of 2 8-bit registers CL and CH, which can be combined together and used as a 16-bit register CX. When combined, CL register contains the low-order byte of the word, and CH contains the high-order byte. Count register can be used as a counter in string manipulation and shift/rotate instructions.

Data register consists of 2 8-bit registers DL and DH, which can be combined together and used as a 16-bit register DX. When combined, DL register contains the low-order byte of the word, and DH contains the high-order byte. Data register can be used as a port number in I/O operations. In integer 32-bit multiply and divide instruction the DX register contains high-order word of the initial or resulting number.

The following registers are both general and index registers:

Stack Pointer (SP) is a 16-bit register pointing to program stack.

Base Pointer (BP) is a 16-bit register pointing to data in stack segment. BP register is usually used for based, based indexed or register indirect addressing.

Source Index (SI) is a 16-bit register. SI is used for indexed, based indexed and register indirect addressing, as well as a source data address in string manipulation instructions.

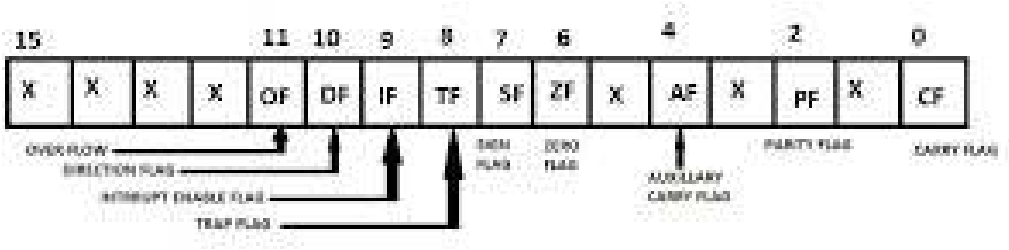
Destination Index (DI) is a 16-bit register. DI is used for indexed, based indexed and register indirect addressing, as well as a destination data address in string manipulation instructions.

Other registers:

Instruction Pointer (IP) is a 16-bit register.

Flags is a 16-bit register containing 9 1-bit flags:

- Overflow Flag (OF) - set if the result is too large positive number, or is too small negative number to fit into destination operand.
- Direction Flag (DF) - if set then string manipulation instructions will auto-decrement index registers. If cleared then the index registers will be auto-incremented.
- Interrupt-enable Flag (IF) - setting this bit enables maskable interrupts.
- Single-step Flag (TF) - if set then single-step interrupt will occur after the next instruction.
- Sign Flag (SF) - set if the most significant bit of the result is set.
- Zero Flag (ZF) - set if the result is zero.
- Auxiliary carry Flag (AF) - set if there was a carry from or borrow to bits 0-3 in the AL register.
- Parity Flag (PF) - set if parity (the number of "1" bits) in the low-order byte of the result is even.
- Carry Flag (CF) - set if there was a carry from or borrow to the most significant bit during last result calculation.



Instruction Set

Instruction set of Intel 8086 processor consists of the following instructions:

- Data moving instructions.
- Arithmetic - add, subtract, increment, decrement, convert byte/word and compare.
- Logic - AND, OR, exclusive OR, shift/rotate and test.
- String manipulation - load, store, move, compare and scan for byte/word.
- Control transfer - conditional, unconditional, call subroutine and return from subroutine.
- Input/Output instructions.
- Other - setting/clearing flag bits, stack operations, software interrupts, etc.

RESULT: Familiarized the 8086 micro processor.

PROGRAMS

1. Addition of two 8-bit numbers.
2. Multiplication of two 8-bit numbers.
3. Addition of two 16-bit numbers.
4. Multiplication of two 16-bit numbers.
5. Even or Odd
6. Factorial of a number.
7. Fibonacci Series
8. Prime Number
9. Searching of an element in a list.
10. Finding the length of a given string.
11. Palindrome.