TED (10)–3066

(REVISION—2010)

Reg. No. .....

Signature .....

THIRD SEMESTER DIPLOMA EXAMINATION IN ENGINEERING/ TECHNOLOGY—MARCH, 2012

DIGITAL COMPUTER PRINCIPLES

(Common for CT, CM and IF)

[*Time :* 3 hours

(Maximum marks : 100)

PART—A

Marks

I Answer all questions. Each question carries 2 marks.

1. Define the term weighted code.
2. Draw the K map for a two input EXOR gate output.
3. Draw the logic symbol for a 2 to 1 multiplexer.
4. Define Race Around Condition in connection with flip-flops.
5. Mention any two applications of shift registers. (5×2=10)

PART—B

II Answer *any five* of the following. Each question carries 6 marks.

1. Define universal property of a gate. Implement AND and OR gates using NAND gates alone.
2. Draw a TTL inverter circuit and briefly explain its working.
3. State the need for a decoder. Design a logic circuit to decode the binary number 1001 for producing a HIGH level at the output.
4. List any three features of sequential circuit.
5. Draw a MOD-8 ripple counter and mention its major disadvantage.
6. Design a 2 bit binary to Gray converter.
7. Multiply the binary numbers 101101 and 1101. Convert the product to octal number. (5×6=30)

PART—C

(Answer *one* full question from each unit. Each question carries 15 marks.)

UNIT—I

III (a) With a suitable example, illustrate the steps to convert a given decimal number to BCD, Gray and Excess-3 codes. 9

(b) Describe the role of alpha numeric codes in digital technology and list any two examples for such codes. 6

OR

Marks

IV (a) Convert the following :
(i) Octal number 723 to decimal
(ii) Decimal number 100 to hexadecimal
(iii) Hexadecimal DE3 to octal
(iv) Decimal number 78 to binary. 10

(b) Differentiate Minterm and Maxterm. 5

UNIT—II

V (a) Using K-map, design a circuit to realize the following expression :
$F(A, B, C, D) = \sum_m (0, 1, 4, 5, 8, 9, 10, 11, 14, 15)$. 12

(b) Define the term fan-out of a logic gate. 3

OR

VI (a) Write short notes on the following terms regarding logic families :
(i) Power dissipation (iii) Propagation delay
(ii) Speed power product (iv) Noise margin. 12

(b) Mention any two advantages of K-mapping method. 3

UNIT—III

VII Draw and explain the working principle of a 4 bit parallel binary adder. Expand it for 8 bit addition. 15

OR

VIII (a) Design a 4 to 1 multiplexer circuit and explain its working. 10

(b) Design a half subtractor circuit. 5

UNIT—IV

IX (a) Explain the working of a 4 bit Serial in Parallel Out and Parallel in Parallel Out shift registers with necessary diagrams. 10

(b) Show how a JK flip-flop is converted to a T-FF and D-FF. 5

OR

X (a) Draw and explain the working principle of a JK flip-flop. 9

(b) Differentiate between synchronous and asynchronous counters. 6