TED (10)–3066

(REVISION—2010)

Reg. No. .....

Signature .....

THIRD SEMESTER DIPLOMA EXAMINATION IN ENGINEERING/ TECHNOLOGY—MARCH, 2014

DIGITAL COMPUTER PRINCIPLES

[Common for CT, CM and IF]

[*Time* : 3 hours

(Maximum marks : 100)

Marks

PART—A

(Maximum marks : 10)

I Answer the following questions in one or two sentences. Each question carries 2 marks.

1. What is weighted code ?
2. What is Karnaugh map ?
3. Define VIL and VIH.
4. List any two applications of a multiplexer.
5. What is a counter ? (5×2=10)

PART—B

(Maximum marks : 30)

II Answer *any five* questions. Each question carries 6 marks.

1. Write short notes on BCD codes.
2. Realize AND and OR gate using NAND gate.
3. State and prove DeMorgan's theorem.
4. Simplify the Boolean expression AB + AB'C + A'BC' + BC'.
5. Design a 1 × 4 demultiplexer with its truth table.
6. Explain RS flip flop with the help of truth table.
7. Write the difference between combinational and sequential logic circuits. (5×6=30)

PART—C

(Maximum marks : 60)

(Answer *one* full question from each unit. Each full question carries 15 marks.)

UNIT—I

III (a) Convert the following binary numbers into decimal and hexa-decimal :

(i) 1011010_2 (ii) 110101101_2 8

(b) Convert the following numbers into octal and binary :

(i) 16489_{10} (ii) 98567_{10} 7

OR

Marks

IV (a) Explain excess–3 code. 8

(b) Explain parity bit for error detection. 7

UNIT—II

V (a) *Define the terms :*

(i) Propagation delay (iii) Fan out

(ii) Noise margin (iv) Power dissipation. 8

(b) Explain the working principle of emitter coupled logic. 7

OR

VI (a) Simplify the Boolean expression A'B'C' + A'BC' + AB'C' + ABC'. 8

(b) Explain with diagram TTL open collector circuit. 7

UNIT—III

VII (a) Explain digital comparator circuit with neat diagram. 8

(b) Explain the operation of a parallel adder with a neat diagram. 7

OR

VIII (a) Explain the working of a full subtractor with neat diagram. 7

(b) Explain the operations of encoder and decoder. 8

UNIT—IV

IX Design and implement a mode-10 ripple counter. 15

OR

X (a) Draw the block diagram, timing diagram and truth table of D Flip flop. 8

(b) Explain the working of a serial in parallel out shift register with diagram. 7

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