MODEL QUESTION PAPER

REVISION-2010
SUB CODE:3066

Reg. No.....
Signature.....

THIRD SEMESTER DIPLOMA EXAMINATION IN ENGINEERING/TECHNOLOGY

DIGITAL COMPUTER PRINCIPLES

(Common to CT, CM, IF)

Time: 3 Hrs. Max. Marks: 100

PART-A

Answer all questions in one or two sentences / words. 2 x 5 = 10

1. Name any code system used to encode computer keyboard input.
2. Draw the logic symbol and truth table for a two input EX-OR gate.
3. Define the term fan-out in connection with logic gate.
4. Write the number of data selector inputs bits required for a 16 to 1 multiplexer.
5. List any two applications of Flip-flops.

PART-B

Answer any 5 questions.. 6 x 5 = 30

6. Draw a 4 bit binary to gray code converter truth table.
7. Realize AND, OR, NOT gates using any universal gate.
8. F(A,B,C)= Σm(0,1,4,5). Simplify the expression using K-Map.
9. Compare TTL and CMOS logic families in terms of fan-in, power dissipation and speed.
10. Design and draw the logic diagram of a half adder using only NAND gates.
11. List any 3 differences between combinational and sequential logic circuits.
12. Draw a 3 bit ripple counter using JK flip flops with truth table.

PART-C

Answer any one question from each module. 15 x 4 = 60

Module 1

13. (i) Explain the term parity bit in data communication system. (5 marks)
    (ii) Find the seven bit Hamming code in even parity scheme for the binary data 1011. (10 marks)

OR

14. (i) Describe briefly about any 3 number systems used in digital systems with examples. (9 marks)
    (ii) Convert the following
    (a) hexadecimal 5A3B to decimal (b) binary 101101 to decimal
    (c) decimal 542 to octal number (6 marks)

Module 2

15. Design and implement 3 bit binary to excess –3 code converter. (15 marks)

OR

16. (i) List any 5 existing logic families. (5 marks)
    (ii) Draw and explai the working of TTL invrter. (10 marks)

Module 3

17.(i) Design the logic circuit for a 4 to 1 multiplexer. (10marks)
(ii) List the various applications of multiplexer. (5 marks)

OR

18. Design a 4 bit Gray to binary code converter with truth table, and logic diagram. (4 marks)

Module 4

19. Explain the working principle of a JK flip-flop with the help of suitable logic diagram, truth table and timing diagram. (15 marks)

OR

20. Design and implement a synchronous counter with counting sequence 0,1,2,3,4,5,0,1 (15marks)