TED (10)–3066

Reg. No. .....

(REVISION—2010)

Signature .....

THIRD SEMESTER DIPLOMA EXAMINATION IN ENGINEERING/ TECHNOLOGY—OCTOBER, 2011

DIGITAL COMPUTER PRINCIPLES

(Common to CT, CM and IF)

[*Time :* 3 hours

(Maximum marks : 100)

PART—A

Marks

I Answer the following questions in one or two sentences. Each question carries 2 marks.

I 1. Convert a given 4 input NAND gate to a 2 input NAND gate.

2. Mention any two advantages of the binary number system.

3. Define De-Morgan's theorem.

4. Half adders are not enough for performing 4 bit binary addition. Give reason.

5. Convert a JK flip-flop to Delay flip-flop. (5×2=10)

PART—B

II Answer *any five* of the following. Each question carries 6 marks.

1. Define Minterm and Maxterm with examples.

2. Prove that $(A\overline{B}\ (C+BD) + \overline{A}\overline{B})\ C = \overline{B}\ C$.

3. Distinguish between decoder and demultiplexer.

4. "The invention of sequential circuits has a great role in the development of computer technology". Justify.

5. Draw a 4 bit Johnson counter using flip-flops, and draw the waveforms.

6. Simplify the expression and draw the logic circuit for the following :
$Y = (A\overline{B} + C\overline{D} + AD)\ D$.

7. Draw a 2 bit parallel binary adder and briefly describe its data movements. (5×6=30)

PART—C

(Answer *one* full question from each unit. Each question carries 15 marks.)

UNIT—I

III (a) List any two differences between octal and hexadecimal number systems. 3

(b) Encode the data 1001 into a seven bit even parity Hamming code. 12

OR

Marks

IV (a) Design an EXOR gate using NAND gates only. 5

(b) Convert the following :

(i) Octal number 632 to hexadecimal

(ii) Decimal 32.46 to binary

(iii) Hexadecimal E0B3 to decimal

(iv) Decimal 83 to octal. 10

UNIT—II

V (a) Design a circuit to realize the following function :

$F(A,B,C,D) = \sum (1,2,6,7,8,9,10,11,13)$. 11

(b) Draw a TTL inverter circuit. 4

OR

VI (a) Differentiate TTL with CMOS logic families. 12

(b) Expand the following :

(i) TTL

(ii) CMOS

(iii) ECL 3

UNIT—III

VII Draw the logic symbol, truth table and design a full subtractor circuit using K mapping. 15

OR

VIII (a) With required diagram, illustrate the working of a BCD to 7 segment driver. 10

(b) Briefly describe the role of a EXOR gate as a basic comparator. 5

UNIT—IV

IX Explain the working of a Master Slave JK flip-flop using NAND gates and the prevention of race around condition. 15

OR

X With necessary diagrams and waveforms, explain the working of an Asynchronous decade counter. 15