TED (10)–3066 Reg. No. .....

(REVISION—2010) Signature .....

THIRD SEMESTER DIPLOMA EXAMINATION IN ENGINEERING/ TECHNOLOGY—OCTOBER, 2013

DIGITAL COMPUTER PRINCIPLES

(Common to CT, CM and IF)

[*Time* : 3 hours

(Maximum marks : 100)

PART—A

(Maximum marks : 10)

Marks

I Answer all questions in one or two sentences. Each question carries 2 marks.

1. What is meant by weighted code ? Give one example.
2. Draw the logic symbol and truth table for a two input EX-OR gate.
3. Define De morgans Theorem.
4. Give any two applications of multiplexer.
5. Draw a serial in serial out shift register. (5×2=10)

PART—B

(Maximum marks : 30)

II Answer *any five* of the following questions. Each question carries 6 marks.

1. Implement AND, OR, NOT gates using NAND gates alone.
2. What is meant by gray code ? Convert the binary no 1001101 to gray code.
3. Express the Boolean expression $F = \overline{A}\,C + \overline{A}\,B + A\overline{B}C + BC$ in sum of minterms.
4. Design a 4 to 1 line multiplexer with truth table.
5. Design a full adder circuit with truth table.
6. List the applications of flip flop.
7. Write the working of a shift register. Differentiate between right shift and left shift registers. (5×6=30)

PART—C

(Maximum marks : 60)

(Answer *one* full question from each unit. Each question carries 15 marks.)

UNIT—I

III (a) Explain the conversion from decimal number to binary number and vice versa with suitable example. 10

(b) Find the seven bit hamming code in even parity scheme for the binary data 1101. 5

OR

Marks

IV (a) Reduce the boolean expression $\overline{A}\,\overline{B} + \overline{A}\,B + A\,B$ using K map. 6

(b) Convert the following :

(i) Hexadecimal 5A3B to decimal

(ii) Binary 1101101 to octal

(iii) Grey code 1101011 to binary. 9

UNIT—II

V (a) Simplify the Boolean function using K map.
$F(x, y, z) = \sum (0, 2, 4, 5, 6)$ 6

(b) Write short notes on the following terms in connection with logic families :

(i) Power dissipation

(ii) Propagation delay

(iii) Noise margin. 9

OR

VI (a) Write the features of CMOS logic gates. 5

(b) Explain the working of TTL inverter with a neat circuit diagram. 10

UNIT—III

VII (a) Write the working of a demultiplexer. Design the circuit for a 1 to 8 line demultiplexer. 10

(b) Draw the logic diagram of a half subtractor with the truth table. 5

OR

VIII (a) Design a full subtractor with circuit diagram and truth table. 10

(b) What is meant by race around condition in flip flops ? 5

UNIT—IV

IX (a) Explain the working principle of a JK flip-flop with the help of logic diagram and truth table. 9

(b) Explain the working principle of ring counter. 6

OR

X Design and implement a mod 10 ripple counter. 15