TED (10)–3068 Reg. No. .....

(REVISION—2010) Signature .....

THIRD SEMESTER DIPLOMA EXAMINATION IN ENGINEERING/ TECHNOLOGY—MARCH, 2014

COMPUTER ARCHITECTURE

(Common for CM, CT and IF)

[*Time* : 3 hours

(Maximum marks : 100)

PART—A

(Maximum marks : 10)

Marks

I Answer all questions in one or two sentences. Each question carries 2 marks.

1. Role of MAR Register.
2. Describe assembler.
3. Name the registers used in the DMA Operation.
4. Write the role of the Cache memory.
5. Functions of Micro program counter. (5×2=10)

PART—B

(Maximum marks : 30)

II Answer *any five* of the following questions. Each question carries 6 marks.

1. Describe pipelining and superscalar operations.
2. Explain the different types of computer.
3. Discuss the steps of interrupt handling.
4. Draw the parallel port interface connection from keyboard to processor.
5. Draw the SRAM cell and explain its parts.
6. Discuss the temporal locality of reference and spatial locality of reference.
7. What is the sequence of operations to add the contents of register R1 to those of R2 and store the result in R3 ? (5×6=30)

PART—C

(Maximum marks : 60)

(Answer *one* full question from each unit. Each full question carries 15 marks.)

UNIT—I

III Explain the functional units of a computer. 15

OR

Marks

IV Discuss the performance of a computer system with the support of basic performance equation. 15

UNIT—II

V (a) Discuss the serial port communication with a diagram. 10

(b) Merits of serial communication. 5

OR

VI (a) Draw and explain the USB structure. 10

(b) Explain the polling scheme in interrupt. 5

UNIT—III

VII (a) Explain single transistor DRAM cell. 10

(b) Describe Memory latency and Memory bandwidth. 5

OR

VIII Explain the magnetic hard disk and its working. 15

UNIT—IV

IX Explain the complete steps involved in execution of instruction Add (R3), R1 with the control sequences. 15

OR

X (a) Explain the hardwired Control Unit Organization. 10

(b) Discuss the role of cache memory in pipelining. 5