MODEL QUESTION PAPER

REVISION-2010
SUB CODE:3068

Reg. No……
Signature……

**THIRD SEMESTER DIPLOMA EXAMINATION IN ENGINEERING/TECHNOLOGY**
**COMPUTER ARCHITECTURE**
(Common to CT, CM and IF)

Time: 3 Hours Max. Marks: 100

## Part A

***I. Answer in One or Two Sentences (5 x 2=10)***

1. State the Basic Performance Equation
2. Write the syntax of any Two Assembler directives.
3. List the different types of ROMs.
4. Name the registers used for the DMA operation.
5. Formulate the control sequence for transferring data from register R1 to R2

## Part B

***II. Answer any 5 questions, (5 x 6 =30)***

1. Describe the sequence of events of data transfer in SCSI.
2. Explain different computer types.
3. Explain the working of Optical Disks.
4. Illustrate the basic concepts of pipelining.
5. Differentiate memory mapped I/O and Peripheral Mapped I/O
6. Explain the functioning of DMA.
7. Draw the architecture of Three Bus Organization

## Part C

***(Answer One full question from each Module. Each full question carries 15 marks.)***

### MODULE I

III a).With a neat diagram explain the functional units of a computer system. (15)

**OR**

IV a). Explain the different factors that affect the performance of a computer system. (15)

### MODULE II

V a). Describe the working of interrupt driven I/O. (6)
b). Explain how it recognizes and handles the multiple interrupt requests. (15)

**OR**

VI a). Explain the Parallel and Serial interfacing circuits. (15)

### MODULE III

VII a). Write notes on
a). Asynchronous DRAM
b). Synchronous DRAM
c) Static RAM (5 x 3 =15)

**OR**

VIII a). With a neat sketch explain organization of virtual memory. (8)
b). Describe the cache memory mechanism. (7)

## MODULE IV

IX a). Explain the steps involved in the execution of instruction ADD (R1), R2, with the control sequences. (15)

**OR**

X a). With necessary block diagrams, explain the organization of hardwired and micro programmed control units. (15)