TED (10)–3068

(REVISION—2010)

Reg. No. .....

Signature .....

THIRD SEMESTER DIPLOMA EXAMINATION IN ENGINEERING/ TECHNOLOGY—OCTOBER, 2012

COMPUTER ARCHITECTURE

(Common for CM, CT and IF)

[*Time :* 3 hours

(Maximum marks : 100)

PART—A

Marks

I Answer the following questions in one or two sentences. Each question carries 2 marks.

1. List the four basic types of operations that need to be supported by an instruction set.
2. State the use of program counter register.
3. Write the function of interrupt vector.
4. Distinguish between temporal locality and spatial locality.
5. Define Control store. (5×2=10)

PART—B

II Answer *any five* of the following. Each question carries 6 marks.

1. State the use of assembler directives. Write any five assembler directives with their syntax and meaning.
2. Give a brief description of pipelining and superscalar operation.
3. Explain the hand-shaked protocol for data transfer over the bus.
4. Discuss the data transfer mechanism of the PCI bus.
5. Write notes on flash memory.
6. Compare static and dynamic RAM.
7. Draw the data path of three bus organization and explain. (5×6=30)

Marks

PART—C

(Answer *one* full question from each unit. Each question carries 15 marks.)

UNIT—I

III Write short notes with necessary diagrams on :

(i) Straight line sequencing

(ii) Branching

(iii) Condition codes. 15

OR

IV (a) With a neat diagram explain the functional units of a computer. 10

(b) Describe the internal registers of the processor. 5

UNIT—II

V Explain DMA and illustrate the direct data transfer between memory and peripherals. 15

OR

VI Explain the Parallel and Serial interfaces. 15

UNIT—III

VII (a) Describe the cache memory mechanism. 7

(b) With a neat diagram describe the internal organization of memory chip. 8

OR

VIII Explain the construction and working of magnetic hard disk. 15

UNIT—IV

IX Explain the steps involved in the execution of instruction MUL R1, (R2), with the control sequences. 15

OR

X (a) Discuss the role of cache memory in pipelining. 3

(b) With necessary block diagram, explain the organization of micro programmed control units. 12