TED (10)–3068 Reg. No. .....

(REVISION—2010) Signature .....

THIRD SEMESTER DIPLOMA EXAMINATION IN ENGINEERING/ TECHNOLOGY—OCTOBER, 2013

COMPUTER ARCHITECTURE

(Common for CM, CT and IF)

[*Time* : 3 hours

(Maximum marks : 100)

Marks

PART—A

I Answer the following questions in one or two sentences. Each question carries 2 marks.

1. Specify the name of two input units.
2. Write the role of Program Counter.
3. Specify the name of two flag/conditional code.
4. Discuss the non-volatile memory.
5. Write the stages of two way pipelining. (5×2=10)

PART—B

II Answer *any five* of the following. Each question carries six marks.

1. Discuss the basic performance equation.
2. Explain multiprocessors and multicomputer.
3. Differentiate memory mapped I/O and I/O mapped I/O.
4. Explain the working of interrupt-service routine.
5. Write notes on flash memory.
6. Explain the internal organisation of memory chips.
7. Discuss the different steps to execute an instruction.

(5×6=30)

PART—C

(Answer one full question from each unit. Each question carries 15 marks.)

UNIT—I

III Explain the basic operational concept of a computer. 15

OR

IV Explain the following :

(i) Straight line sequencing (ii) Branching (iii) Conditional codes. 15

Marks

UNIT—II

V (a) Discuss the DMA data transfer. 9

(b) Explain synchronous Bus with timing of input transfer. 6

OR

VI (a) Draw and explain the USB structure. 10

(b) Explain the polling scheme in interrupt. 5

UNIT—III

VII (a) Explain SRAM cell. 10

(b) Describe Memory latency and Memory bandwidth. 5

OR

VIII Explain the virtual memory and its working. 15

UNIT—IV

IX (a) Explain the complete steps involved in execution of an unconditional branch instruction with the control sequences. 10

(b) Write the role of cache memory in pipelining. 5

OR

X (a) Explain the micro programmed Control Unit Organization. 10

(b) Draw a multiple-Bus Organization. 5