TED (10)–3068

(REVISION—2010)

Reg. No. .....

Signature .....

THIRD SEMESTER DIPLOMA EXAMINATION IN ENGINEERING/ TECHNOLOGY—MARCH, 2012

COMPUTER ARCHITECTURE

(Common to CT, CM and IF)

[*Time* : 3 hours

(Maximum marks : 100)

Marks

PART—A

I Answer *all* questions in one or two sentences. Each question carries 2 marks.

1. Expand CISC and RISC.
2. Write the functions of ALU.
3. Define Interrupt Service Routines.
4. Define locality of reference.
5. Write the control sequence for storing the value from a register to main memory. (5x2=10)

PART—B

II Answer *any five* of the following questions. Each question carries 6 marks.

1. Write notes on : (i) Multiprocessors (ii) Multi computers.
2. Explain the steps involved in assembling and execution of a program.
3. Differentiate between Memory mapped I/O and Peripheral mapped I/O.
4. Write the characteristics of : (i) Synchronous bus (ii) Asynchronous bus.
5. Explain the working of magnetic tape systems.
6. Draw the architecture of three bus organization.
7. Write the advantages and disadvantages of microprogrammed control unit. (5x6=30)

PART—C

(Answer *one* full question from each unit. Each question carries 15 marks.)

UNIT – I

III With a neat diagram explain the functional units of a computer system. 15

Or

Mark

UNIT – II

V Explain the parallel and serial interfacing circuits. 15

OR

VI Write notes on : (i) PCI (ii) SCSI (iii) USB (3x5=15)

UNIT – III

VII With a diagram, explain the structure of connecting many memory chips to form a large memory. 15

OR

VIII (a) Explain the working of magnetic hard disks with a diagram. 8

(b) Describe the cache memory mechanism. 7

UNIT – IV

IX Explain the steps involved in the execution of instruction ADD (R1), (R2) with the control sequences. 15

OR

X (a) Explain about Hardwired control unit. 9

(b) Explain the role of cache memory in pipelining. 6