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(Revision 2010)

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THIRD SEMESTER DIPLOMA EXAMINATION IN ENGINEERING/ TECHNOLOGY - MARCH 2013

DIGITAL COMPUTER PRINCIPLES

Common to CT, CM, IF)

[Total Marks: 100] [Time: 3 Hours]

PART- A

(Maximum Marks: 10)

Marks

I. Answer all questions in one or two sentences. Each question carries 2 marks)

1. Write the features of binary number system.
2. Distinguish between positive and negative logic.
3. Write the basic principle of Karnaugh map.
4. Distinguish between decoder and demultiplexer.
5. Write any two applications of shift registers. (5x2=10)

PART – B

(Maximum Marks: 30)

II. Answer any five of the following questions. Each question carries 6 marks.

1. Draw the truth table and logic symbol for an EX-OR and EX-NOR gates.
2. Expand A+B to min terms and max terms.
3. Explain the working of a TTL inverter circuit with diagram.
4. Design the logic diagram of a 1 to 4 line demultiplexer and write the truth table.
5. Design and draw the logic diagram of a half subtractor using only NAND gates.
6. Explain working principle of ring counter.
7. Distinguish between combinational circuit and sequential circuit.

(5x6=30)

PART - C

(Maximum Marks: 60)

(Answer one full question from each unit. Each question carries 15 marks)

UNIT-I

III. a. Explain BCD code, excess-3 code and Gray code with examples (9)

b. Multiply the binary numbers 10101 and 1001, Convert the product to hexa decimal number. (6)

OR

IV. a. State the universal property of a gate, Realize AND, OR, NOT gates using any universal gate. (11)

b. Convert the following (i) $(1101.11)_2$ to decimal (ii) $(7324)_8$ to hexadecimal (4)

UNIT-II

V. a. Explain why ECL is consider as the fastest of all logic families. Write their characteristics and draw backs. (9)

b. List the advantages and disadvantages of Karnaugh map. (6)

OR

VI a. Simplify the Boolean function using K Map. $F(x, y, z) = \Sigma (3, 4, 6, 7)$ (5)

b. Compare CMOS and TTL logic families. (10)

UNIT – III

VII. a. Design the logic circuit for a 4 to 1 multiplexer and explain its working. (9)

b. Distinguish parallel addres and serial addres . (6)

OR

VIII. a. Explain the role of an EX NOR gate as a basic comparator. (5)

b. Design the logic circuit for a 2 to 4 line decoder and explain its working. (10)

UNIT – IV

IX. a. Explain the shift register with the help of suitable logic diagram. (9)

b. Explain the working of clocked SR flip flop with suitable diagram and truth table. (6)

OR

X. a. Explain the working principle of a master salve JK flip-flop with the help of suitable logic diagram and truth table. (10)

b. Distinguish between synchronous and asynchronous counters. (5)