MODEL QUESTION PAPER

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THIRD SEMESTER DIPLOMA EXAMINATION IN ELECTRICAL & ELECTRONICS ENGINEERING, OCTOBER 2011
ELECTRONIC DEVICES AND CIRCUITS

Time :3hours Maximum marks:100

PART A (maximum marks 10)

I. Answer the following questions in 2 or 3 sentences: marks

1A. The depletion region has immobile ions which are electrically charged.This electric field between the acceptor and donor ions is called a a barrier.Due to this electric field a potential is established between P and N region which is called potential barrier

2A. Given $I_B = 20\ \mu A$

$\beta = 50$

we know $I_C / I_B = \beta$

$\therefore I_C = I_B \beta = 20 \times 50 = 1000\ \mu A$

Then $I_E = I_C + I_B$

$I_E = 1000 + 20 = 1020\ \mu A$

3A.The difference between two cut off frequencies is called bandwidth. BW=(F2-F1),where f2 and F1 are upper and lower cutoff frequencies respectively.

4A.RC coupling and transformer coupling.

5A. (i) The loop gain $|A\beta| = 1$

(ii) The total phase shift around the loops is 0^0 (or an integral multiple of 360^0). In other words, feedback should be positive.

PART B (Maximum marks :30)

II Answer any five questions from the following

1A

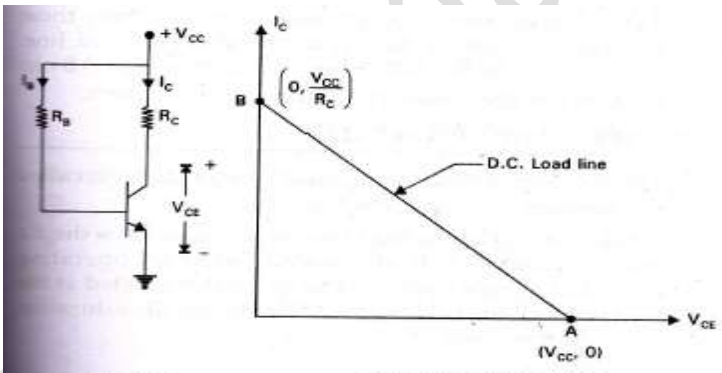


Fig. 1.30

Fig. 1.31 DC Load Line

The values of V_{CC} and R_C are fixed and I_C and V_{CE} are dependent on R_B.

Applying KVL to the collector circuit, we get

$$V_{CC} = I_C R_C + V_{CE} \quad \ldots (1)$$

(or) $$I_C = -\frac{1}{R_C} V_{CE} + \frac{V_{CC}}{R_C} \quad \ldots (2)$$

(i) If $I_C = 0$, then $V_{CE} = V_{CC}$

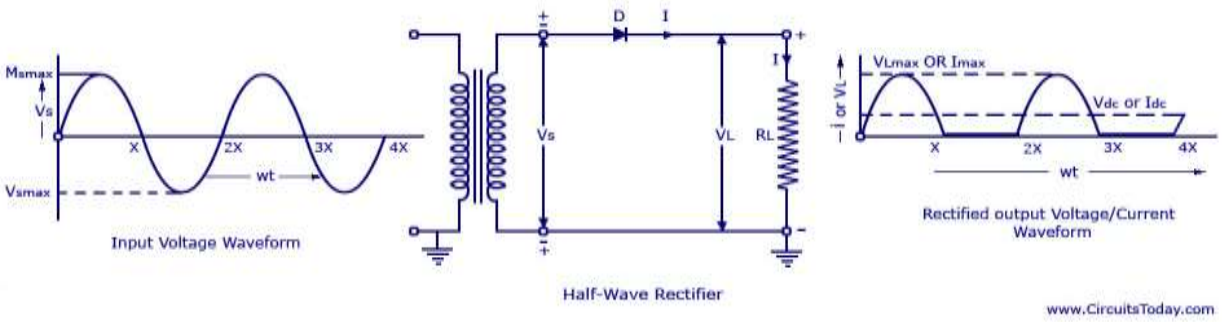
This gives the point, A = $(V_{CC}, 0)$

At point A, the transistor is in cut off condition.

(ii) If $V_{CE} = 0$, then $I_C = \frac{V_{CC}}{R_C}$

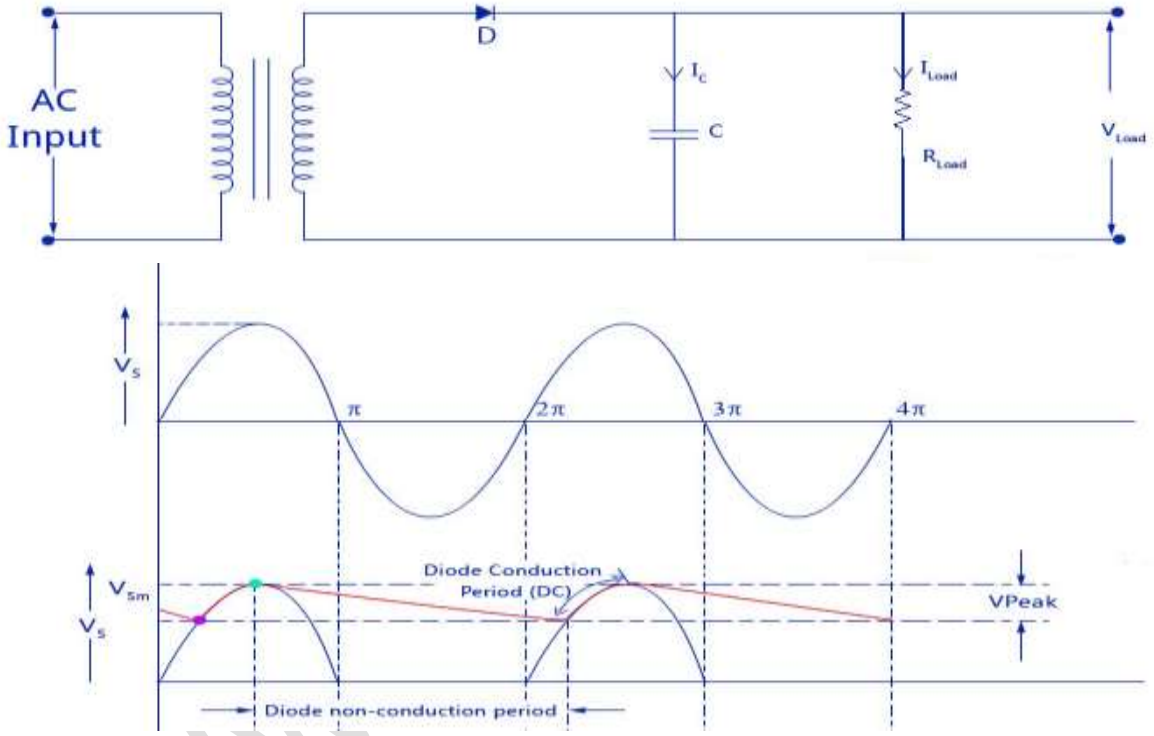
This gives the point, B = $\left(0, \frac{V_{CC}}{R_C}\right)$.

2A.



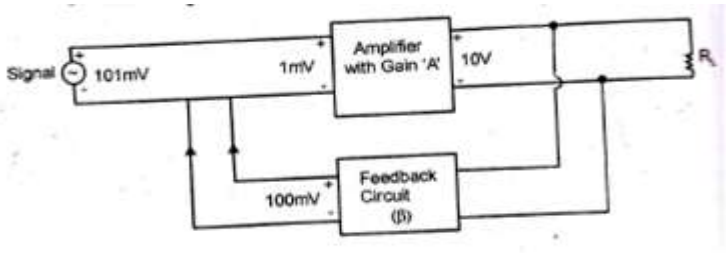
The input we give here is an alternating current. This input voltage is stepped down using a transformer. The reduced voltage is fed to the diode 'D' and load resistance RL. During the positive half cycles of the input wave, the diode 'D' will be forward biased and during the negative half cycles of input wave, the diode 'D' will be reverse biased. We take the output across load resistor RL. Since the diode passes current only during one half cycle of the input wave, we get an output as shown in diagram. The output is positive and significant during the positive half cycles of input wave. At the same time output is zero or insignificant during negative half cycles of input wave. This is called half wave rectification.

3A.



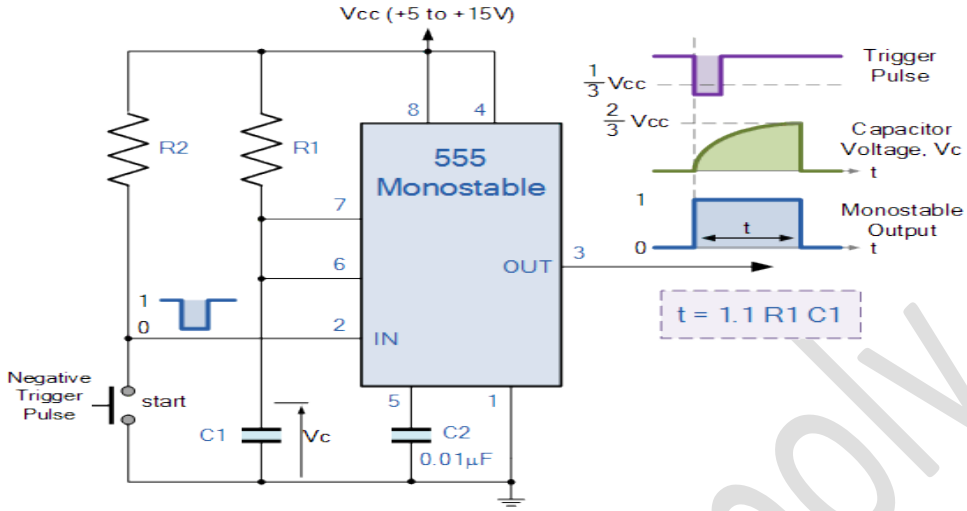
During the positive half cycle of the input ac voltage, the diode D will be forward biased and thus starts conducting. During this period, the capacitor 'C' starts charging to the maximum value of the supply voltage Vsm. When the capacitor is fully charged, it holds the charge until the input ac supply to the rectifier reaches the negative half cycle. As soon as the negative half supply is reached, the diode gets reverse biased and thus stops conducting. During the non-conducting period, the capacitor 'C' discharges all the stored charges through the output load resistance RLoad. As the voltage across RLoad and the voltage across the capacitor 'C' are the same (VLoad = Vc), they decrease exponentially with a time constant (C*RLoad) along the curve of the non-conducting period.

4A. when any increase in the output signal results in a feedback signal into the input in such a way as to decrease the output signal the amplifier is said to have negative feedback.The output of the amplifier is 10v.The fraction beta of this output ie 100mV is feedback to the input where it is applied in series with the input signal of 101mV.As the feedback is negative only 1mV appears At the input terminals of the amplifier.

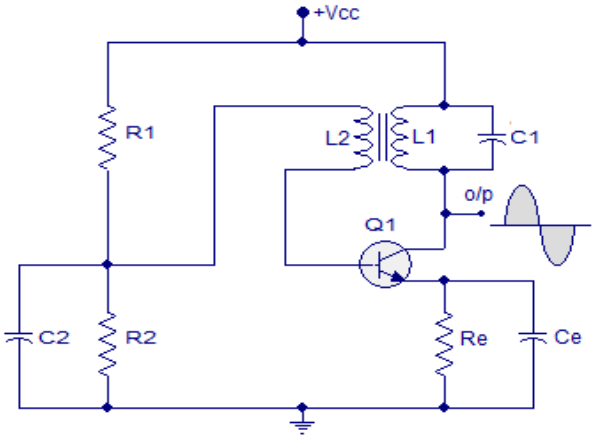


$$G = \frac{A}{1 + \beta A}$$

5A



6A



Tuned collector oscillator

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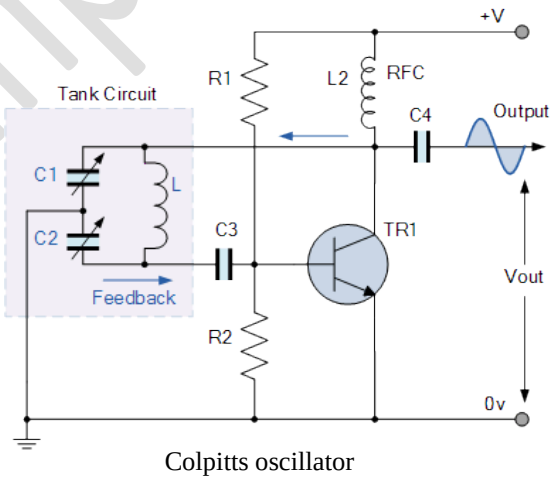
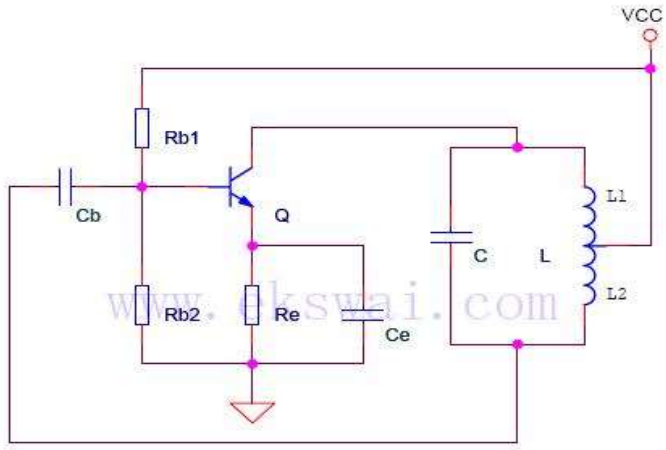


Colpitts oscillator



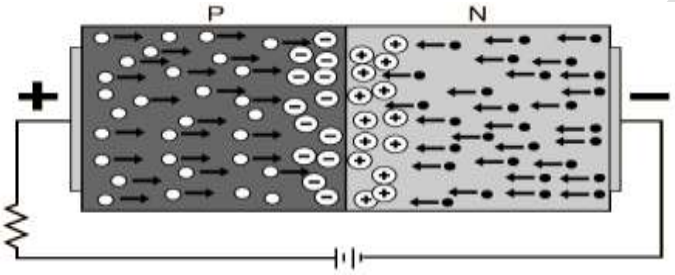
Hartley oscillator

7A.

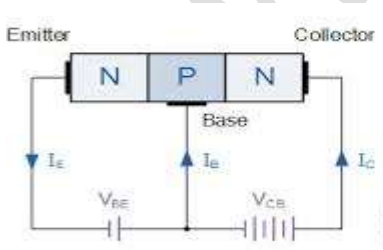
Ordinary Diode	Zener Diode
(*) Current conducts only in one direction	(*) Allows the conduction in both directions
(*) The diode will be Permenently damaged for a large reverse current.	(*) It will not damage
(*) Diode are normally used for rectification	(*) Zener diode are used for voltage regulation.
	

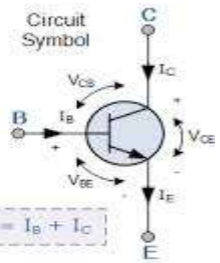
PART C

111 (a) If an external voltage is connected in such a way that the P region terminal is connected to the positive of DC voltage and the N region is connected to the negative of the DC voltage, the biasing condition is called forward biasing. When we apply an external voltage more than the barrier potential, the negative terminal of battery pushes the electrons against barrier from N to P region. Similarly positive terminal pushes the holes from P to N region. Thus holes get repelled by positive terminal and cross the junction against barrier potential. This reduces the width of depletion region. As forward voltage increased, at a particular value the depletion region becomes very much narrow such that large number of charge carriers can cross the junction.In this way the flow of charge increases through the diode by increasing the applied voltage. The motion of charge particles can be observed in below picture.



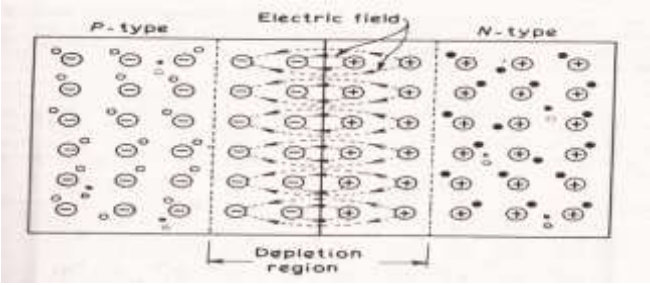
(a) Potential is applied across the base/emitter junction this makes the base/emitter junction forward biased.A much higher potential is applied across the base/collector junction with a relatively high positive voltage applied to the collector, so that the base/collector junction is heavily reverse biased. This makes the depletion layer between base and collector . When the base emitter junction is forward biased, a small current will flow into the base. Therefore holes are injected into the P type material. These holes attract electrons across the forward biased base/emitter junction to combine with the holes.Because the emitter region is very heavily doped, many more electrons cross into the base region than are able to combine with holes. This means there is a large concentration of electrons in the base region and most of these electrons are swept straight through the very thin base and enters in to the collector material.Varying the current flowing into the base, affects the number of electrons attracted from the emitter. In this way very small changes in base current cause very large changes in the current flowing from emitter to collector, so current amplification is taking place.



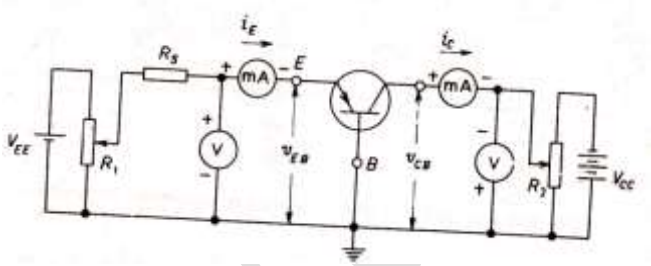


$$I_E = I_B + I_C$$

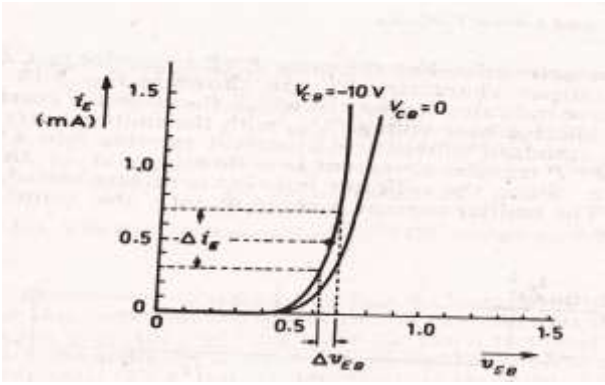
1V (a) Holes from the P region diffuse into the N region. Then they combine with the electrons in the N region. Free electrons from the N region diffuse into the P region. These electrons will combines with the holes. After a few recombination then a restraining force will develop automatically called barrier. Further diffusion is stopped by this barrier. Some of the holes in the P region and some of the free electrons in N region diffuse towards each other and recombine. Each recombination eliminates a hole and a free electron. The –ve acceptor ions in the P region and +ve donor ions in N region are left uncompensated. The region containing the uncompensated acceptor and donor ions is called depletion region or space charge region. The electric field between the acceptor and donor ions is called a barrier.



(b) **common base configuration :** It is plotted between Veb and Ie ,making Vcb constant..The emitter base junction is forward biased,when the Vcb increases the curve resembles like a diode.



Input characteristics of common base (CB):

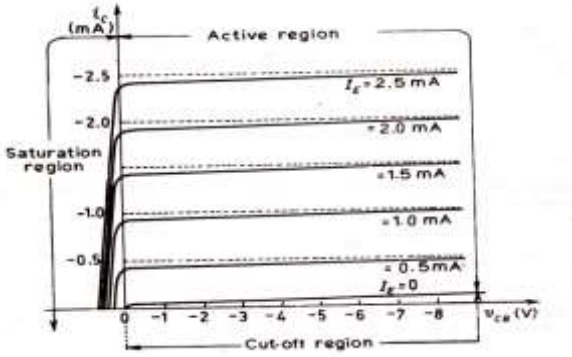


$$r_i = \frac{\Delta V_{EB}}{\Delta I_E}\Big|_{V_{CB}=\text{constant}}$$

Output characteristics of common base (CB): The collector current Ic is approximately equal to the emitter current Ie

.In active region ,the curve are almost flat.This shows that Ic increases only slightly as Vcbinctreases.

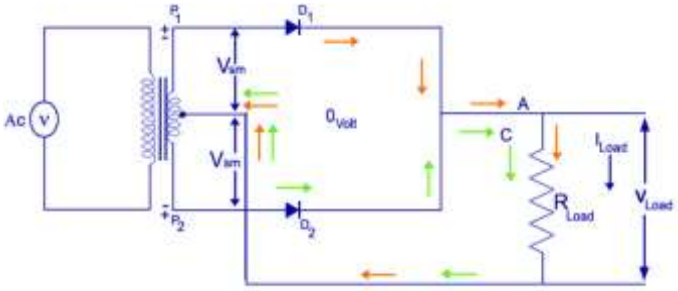
.As Vcb becomes +ve the collector current Ic sharply decreases.This is the saturation region.In this region the collector doesnot depend much upon the emitter current..



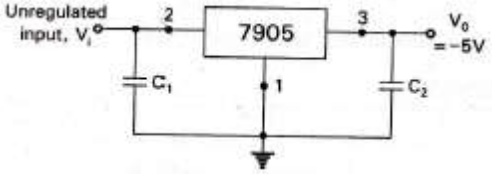
.The collector current is not zero when Ie=0.It has a small value.This is the reverse leackage current Ico

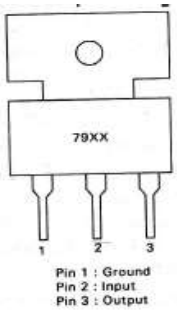
(V) In the case of centre-tap full wave rectifier, only two diodes are used, and are connected to the opposite ends of a centre-tapped secondary transformer as shown in the figure below. The centre-tap is usually considered as the ground point or the zero voltage reference point An ac input is applied to the primary coils of the transformer. This input makes the secondary ends P1 and P2 become positive and negative alternately. For the positive half of the ac signal, the secondary point D1 is positive, GND point will have zero volt and P2 will be negative. At this instant diode D1 will be forward biased and diode D2 will be reverse biased.

the diode D1 will conduct and D2 will not conduct during during the positive half cycle. Thus the current flow will be in the direction P1-D1-C-A-B-GND. Thus, the positive half cycle appears across the load resistance RLOAD.During the negative half cycle, the secondary ends P1 becomes negative and P2 becomes positive. At this instant, the diode D1 will be negative and D2 will be positive with the zero reference point being the ground, GND. Thus, the diode D2 will be forward biased and D1 will be reverse biased. The diode D2 will conduct and D1 will not conduct during the negative half cycle. The current flow will be in the direction P2-D2-C-A-B-GND.

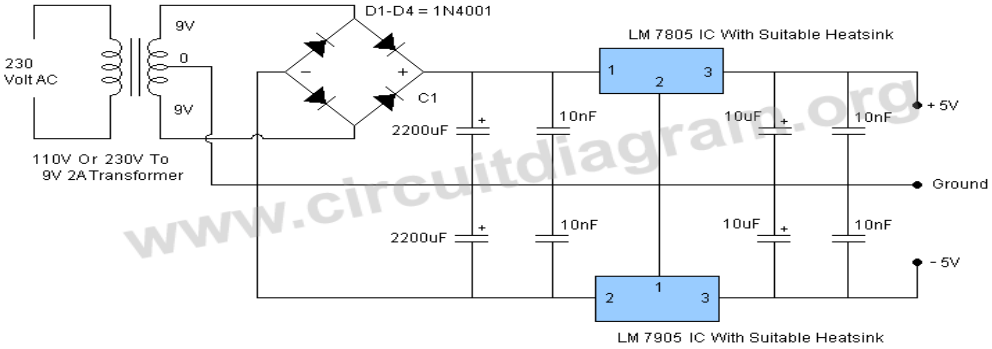


(a)

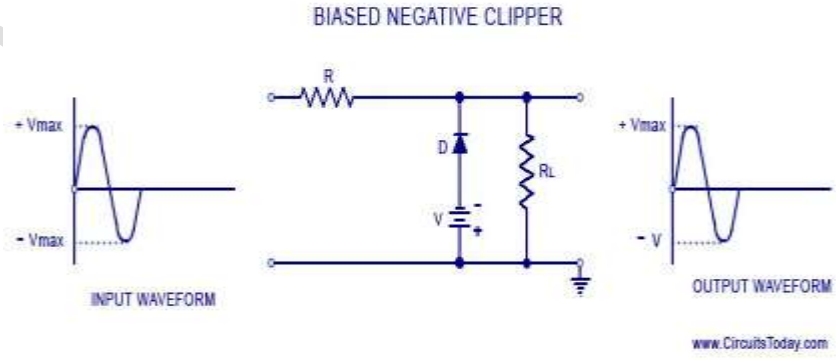




pin 2 is the input terminal, pin 1 is the ground and pin 3 is the output terminal. The unregulated input voltage (V1) is given to the input terminal. The output is taken from the output terminal. Filter capacitors are shown to be connected at the input and output side. The input capacitor C1 is used to cancel the inductive effects due to long distiibution leads and the output capacitor C2 improves the transient response.

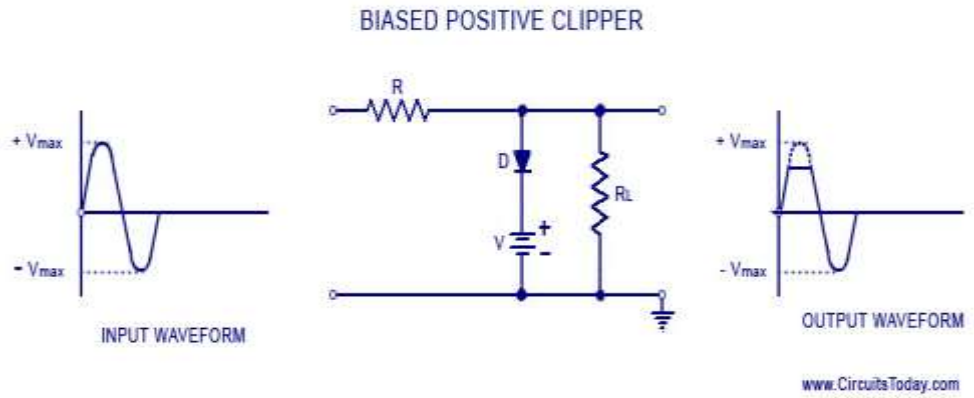


(a) A biased clipper comes in handy when a small portion of positive or negative half cycles of the signal voltage is to be removed. When a small portion of the negative half cycle is to be removed, it is called a biased negative clipper.

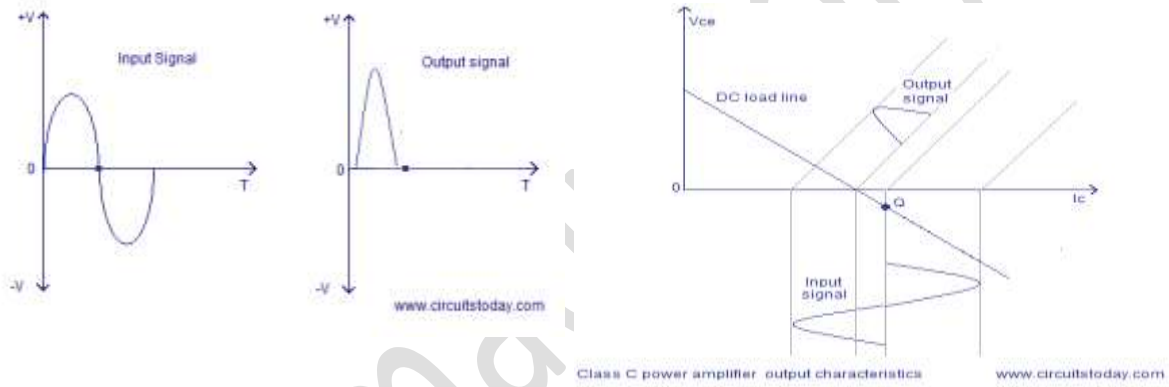


when the input signal voltage is positive, the diode ‘D’ is reverse-biased. This causes it to act as an open-switch. Thus the entire positive half cycle appears across the load, as illustrated by output waveform .When the input signal voltage is negative but does not exceed battery the voltage ‘V’, the diode ‘D’ remains reverse-biased and most of the input voltage appears across the output.

When during the negative half cycle of input signal, the signal voltage becomes more than the battery voltage V, the diode D is forward biased and so conducts heavily. The output voltage is equal to '- V' and stays at '- V' as long as the magnitude of the input signal voltage is greater than the magnitude of the battery voltage, 'V'. Thus a biased negative clipper removes input voltage when the input signal voltage becomes greater than the battery voltage.



V11 (a) Class C power amplifier is a type of amplifier where the active element (transistor) conduct for less than one half cycle of the input signal. Less than one half cycle means the conduction angle is less than 180° and its typical value is 80° to 120°. The reduced conduction angle improves the efficiency to a great extend but causes a lot of distortion. Theoretical maximum efficiency of a Class C amplifier is around 90%.



Advantages of Class C power amplifier.

- High efficiency.,Excellent in RF applications.,Lowest physical size for a given power output.

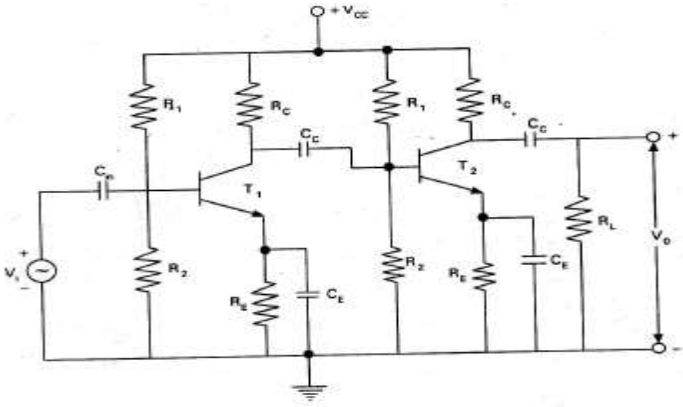
Disadvantages of Class C power amplifier.

- Lowest linearity,Not suitable in audio applications.,Creates a lot of RF interference,It is difficult to obtain ideal inductors and coupling transformers,Reduced dynamic range.

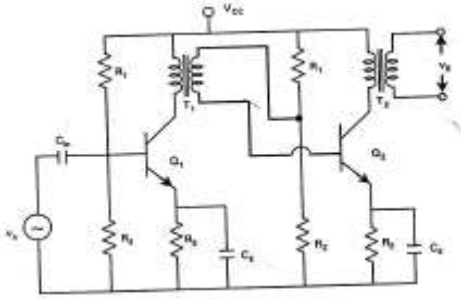
Applications of Class C power amplifier.

- RF oscillators,RF amplifier,FM transmitters,Booster amplifiers,High frequency repeaters,Tuned amplifiers etc.

(a) Various coupling schemes are RC coupling,transformer coupling,direct coupling and impedence coupling.

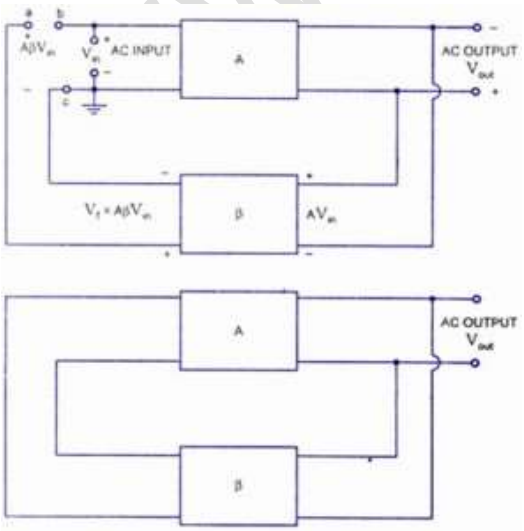


When an ac signal is applied to the input of tirst stage, it gets amplified by this stage and appears across the collector resistor itc of first-stage: This output voltage of first-stage is coupled to the base of the second stage through the coupling capacitor C. The amplified signal of first stage gets further amplification by the second stage and hence more amplification takes place. The output of the stage is taken out through the coupling The overall gain of amplification is equal so product of the individual stage gains. A, - Ay, x A; It Is to be noted that as the configuration employed Is CE configuration, each stage of amplification produces a phase shift of the input signal by 1W. The overall phase shift is 2 x 1130,or 360° or there's no phase difference between the input signal and the output of the second stage of amplification.



The input ac signal is applied to the base of the first stage transistor. It is amplified by the first stage and appears across the primary winding of the transformer T,. The amplified ac voltage across the primary winding of T, is transferred to the secondary winding,by induction and is given to the input of the second stage. It ls further amplified by the second stage amplifier. The output appears across the secondary winding of transformer, T2

V111 (a) A feedback amplifier having closed-loop gain, A_f greater than unity can be obtained by the use of a positive feedback. This result also satisfies the phase condition and thus results in the operation of an oscillator circuit. An oscillator circuit then provides a constantly varying output signal. If the output signal varies sinusoidally, the circuit can be called as a sinusoidal oscillator. The amplified output voltage is $\mathbf{V_{out} = A\ V_{in}}$This voltage drives a feedback circuit that is usually a resonant circuit, as we get maximum feedback at one frequency. The feedback voltage returning to point a is given by equation $\mathbf{V_f = A\ \beta\ V_{in}}$ **where β is the gain of feedback network**.If the phase shift through the amplifier and feedback circuit is zero, then A β V_{in} is in phase with the input signal V_{in} that drives the input terminals of the amplifier.Certain conditions are required to be fulfilled for sustained oscillations and these conditions are that

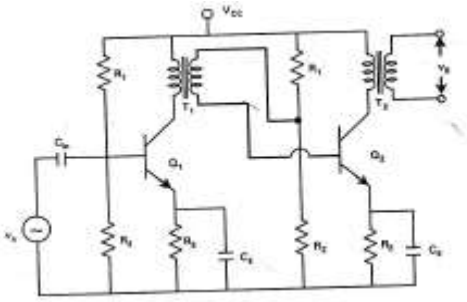


(i) The loop gain of the circuit must be equal to (or greater than) unity and

(ii) The phase shift around the circuit must be zero. These two conditions for sustained oscillations are called Barkhausen *criteria*.

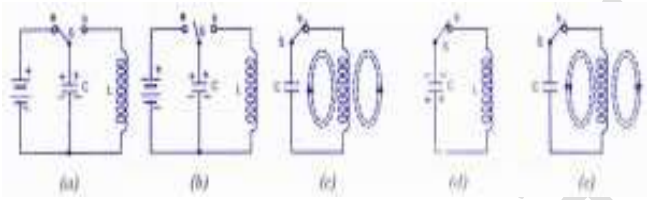
Applications: used in oscillators such as LC oscillators,colpitts,rc phase shift,crystal oscillators etc.

(b) The input ac signal is applied to the base of the first stage transistor. It is amplified by the first stage and appears across the primary winding of the transformer T,. The amplified ac voltage across the primary winding of T, is transferred to the secondary winding,by induction and is given to the input of the second stage. It ls further amplified by the second stage amplifier. The output appears across the secondary winding of transformer, T2



Applications: used in radio and TV receivers for amplifying signals.it is used in power amplifiers

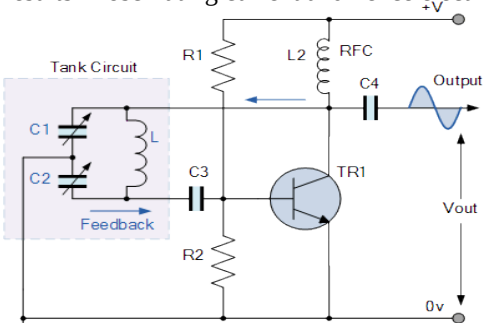
1X (a) conditions are required to be fulfilled for sustained oscillations and these conditions are that The loop gain of the circuit must be equal to (or greater than) unity and The phase shift around the circuit must be zero. These two conditions for sustained oscillations are called Barkhausen *criteria*.



let the capacitor be charged from a dc source with the polarity as shown in figure (a). A potential difference will be across the plates of the capacitor because of the accumulation of electrons in the lower plate of the capacitor. The electrons get accumulated in the lower plate due to the supply from the negative terminal of the battery. Thus, a potential energy will be formed in the capacitor. Now when the capacitor is fully charged and the switch S is opened, as shown in figure (b), the capacitor cannot discharge through L.

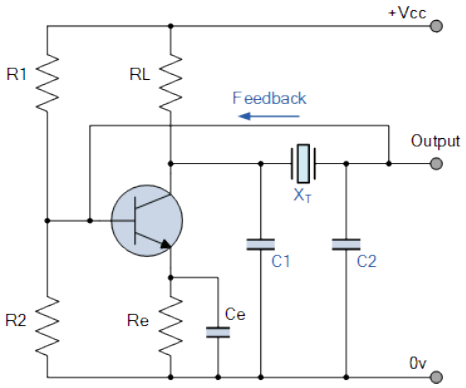
Suppose the switch S is kept in position 'b'. The current starts flowing in the circuit but the self induced emf in the coil opposes the current flow. Thus the rate of rise of current is slow. Maximum current flows in the circuit when the capacitor is fully discharged. Due to flow of current, magnetic field is set up which stores the energy given by the electric field,as shown in figure (c). Thus, at the instant the capacitor gets completely discharged, the electrostatic energy stored in the capacitor gets converted into the magnetic field energy associated with the inductor L.When the capacitor is completely discharged, the magnetic field begins to collapse and a counter or back emf is developed which, according to Lenz's law, keeps the current flowing in the same direction. The capacitor now starts getting charge but with opposite polarity, as shown in fig.(d). In this case, the energy associated with the magnetic field is again converted into electrostatic energy. In an ideal case (that is, both the L and C are loss-free), the capacitor is charged to the value it had initially while the magnetic field energy reduces to zero.After the collapsing field has recharged the capacitor, the capacitor now begins to discharge with a current flow in the opposite direction. The electric field starts collapsing whereas magnetic field starts building up again but in opposite direction. Fig. (e) shows the condition when the capacitor gets fully discharged. The sequence of charging and discharging continues, that is, the process of transformation of dielectric energy into magnetic energy and vice-versa is repeated again and again. This situation is similar to an oscillating pendulum, in which the energy keeps on interchanging between potential and kinetic energy. Thus the charge and discharge of a capacitor through inductor results in oscillating current and hence electrical oscillations are set up in the L-C or tank circuit.

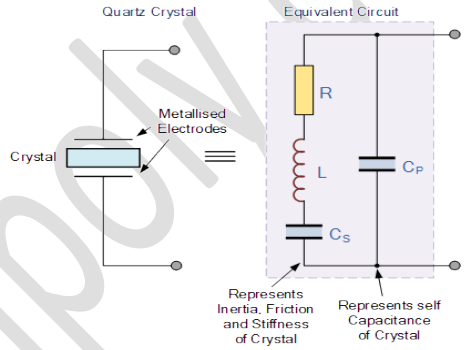
(b)



The transistor amplifiers emitter is connected to the junction of capacitors, C1 and C2 which are connected in series and act as a simple voltage divider. When the power supply is firstly applied, capacitors C1 and C2 charge up and then discharge through the coil L. The oscillations across the capacitors are applied to the base-emitter junction and appear in the amplified at the collector output.The amount of feedback depends on the values of C1 and C2 with the smaller the values of C the greater will be the feedback.The required external phase shift is obtained in a similar manner to that in the Hartley oscillator circuit with the required positive feedback obtained for sustained un-damped oscillations. The amount of feedback is determined by the ratio of C1 and C2. These two capacitances are generally "ganged" together to provide a constant amount of feedback so that as one is adjusted the other automatically follows.

X (a) These types of **Crystal Oscillators** are designed around the common emitter amplifier stage of a **Colpitts Oscillator**. The input signal to the base of the transistor is inverted at the transistors output. The output signal at the collector is then taken through a 180^o phase shifting network which includes the crystal operating in a series resonant mode.The output is also fed back to the input which is "in-phase" with the input providing the necessary positive feedback. Resistors, R1 and R2 bias the resistor in a Class A type operation while resistor Re is chosen so that the loop gain is slightly greater than unity.Capacitors, C1 and C2 are made as large as possible in order that the frequency of oscillations can approximate to the series resonant mode of the crystal and is not dependant upon the values of these capacitors.The circuit diagram above of the **Colpitts Crystal Oscillator** circuit shows that capacitors, C1 and C2 shunt the output of the transistor which reduces the feedback signal. Therefore, the gain of the transistor limits the maximum values of C1 and C2.





The output amplitude should be kept low in order to avoid excessive power dissipation in the crystal otherwise could destroy itself by excessive vibration.

(b)

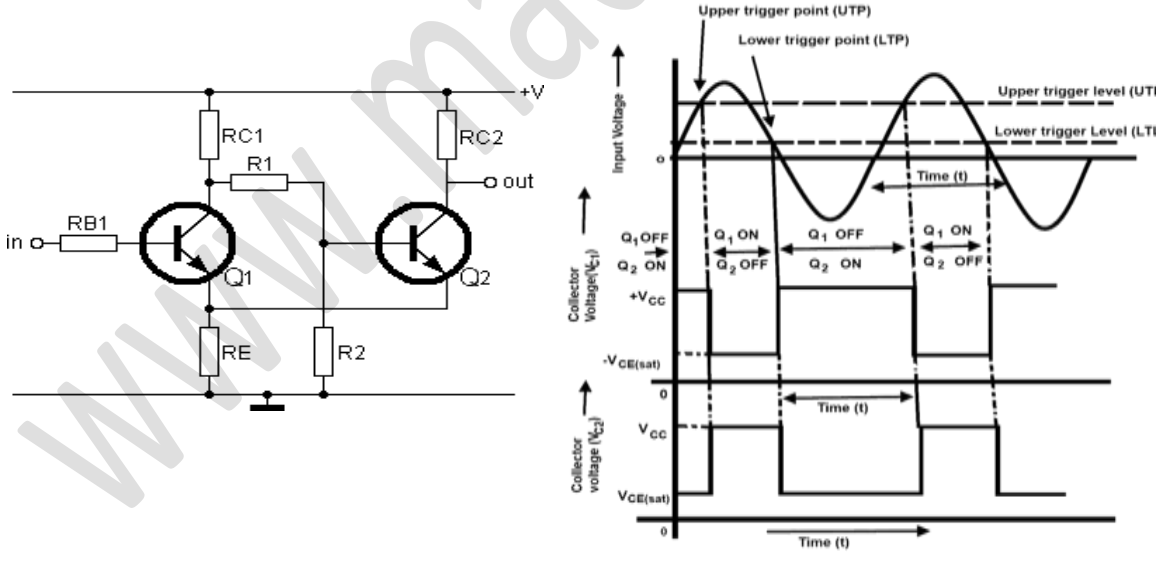


Figure 2: Waveforms at the input and collector of transistor Q1 and Q2

A.C. signal is applied at the input of the Schmitt trigger (i.e. at the base of the transistor Q_1). As the input voltage increases above zero, nothing will happen till it crosses the upper trigger level (U.L.T). As the input voltage increases, above the upper trigger level, the transistor Q_1 conducts. The point, at which it starts conducting, is known as upper trigger point (U.T.P). As the transistor Q_1 conducts, its collector voltage falls below V_{CC}. This fall is coupled through resistor R_1 to the base of transistor Q_2 which reduces its forward bias. This in turn reduces the current of transistor Q_2 and hence the voltage drop across the resistor R_E. As a result of this, the reverse bias of transistor Q_1 is reduced and it conducts more. As the transistor Q_1 conducts more heavily, its collector further reduces due to which the transistor Q_1 conducts near cut-off. This process continues till the transistor Q_1 is driven into saturation and Q_2 into cut-off. At this instant, the collector voltage levels are $V_{C1} = V_{CE(sat)}$ and $V_{C2} = V_{CC}$ as shown in the figure.The transistor Q_1 will continue to conduct till the input voltage falls below the lower trigger level (L.T.L). It will be

interesting to know that when the input voltage becomes equal to the lower trigger level, the emitter base junction of transistor Q_1 becomes reverse biased. As a result of this, its collector voltage starts rising toward V_{CC}. This rising voltage increases the forward bias across transistor Q_2 due to which it conducts. The point, at which transistor Q_2 starts conducting, is called lower trigger point (L.T.P). Soon the transistor Q_2 is driven into saturation and Q_1 to cur-off. This completes one cycle. The collector voltage levels at this instant are $V_{C1} = V_{CC}$ and $V_{C2} = V_{CE(sat)}$. No change in state will occur during the negative half cycle of the input voltage.