REVISION-2010 Reg. No

SUB CODE:3053 Signature

THIRD SEMESTER DIPLOMA EXAMINATION IN ELECTRICAL & ELECTRONICS ENGINEERING, MARCH 2013

ELECTRONIC DEVICES AND CIRCUITS

Time :3hours Maximum marks:100

PART A

(maximum marks 10)

I. Answer the following questions in 2 or 3 sentences:

1A the charge carriers have the tendency to move from the region of higher concentration to that of lower concentration of the same type of charge carriers. Thus the movement of charge carriers takes place resulting in a current called diffusion current

2A rectifier,detector

3A It is the maximum value of reverse voltage which occurs at the peak of the input cycle when the diode is reverse-biased.

4A faithful amplification is the amplification of a signal, particularly a weak one, by a triode or a transistor such that the signal changes in amplitude but not in shape.

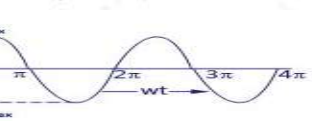
5A positive feedback, the phase near the circuit needs to be either 360 or zero degrees, and the loop gain should be equal or greater than 1

PART B (Maximum marks :30)

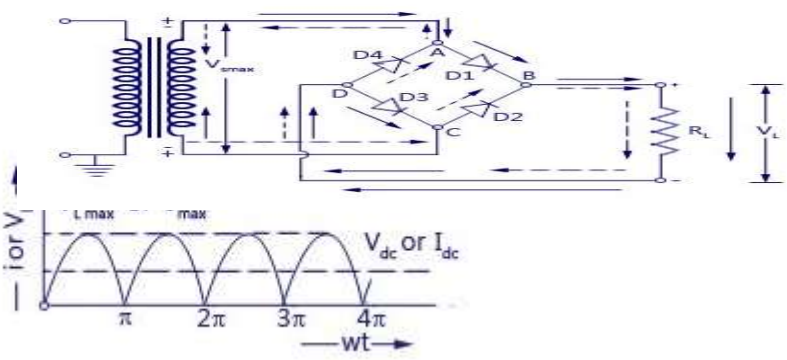
II Answer any five questions from the following

1A

Ordinary Diode	Zener Diode
(*) Current conducts only in one direction (*) The diode will be Permanently damaged for a large reverse current. (*) Diode are normally used for rectification	(*) Allows the Conduction in both directions (*) It will not damage (*) Zener diode are used for voltage regulation.



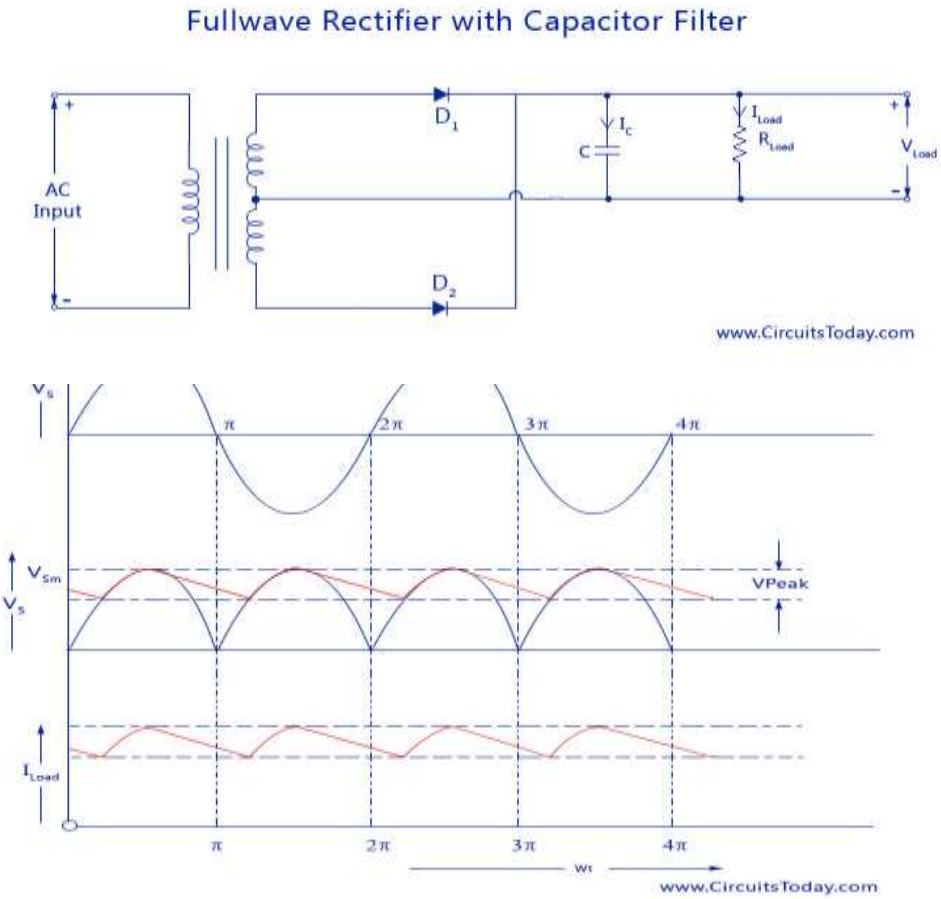
Input Voltage Waveform



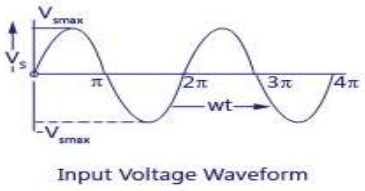
During first half cycle of the input voltage, the upper end of the transformer secondary winding is positive with respect to the lower end. Thus during the first half cycle diodes D1 and D_3 are forward biased and current flows through arm AB, enters the

load resistance R_L, and returns back flowing through arm DC. During this half of each input cycle, the diodes D_2 and D_4 are reverse biased and current is not allowed to flow in arms AD and BC. The flow of current is indicated by solid arrows in the figure above. We have developed another diagram below to help you understand the current flow quickly. During second half cycle of the input voltage, the lower end of the transformer secondary winding is positive with respect to the upper end. Thus diodes D_2 and D_4 become forward biased and current flows through arm CB, enters the load resistance R_L, and returns back to the source flowing through arm DA. Flow of current has been shown by dotted arrows in the figure. Thus the direction of flow of current through the load resistance R_L remains the same during both half cycles of the input supply voltage

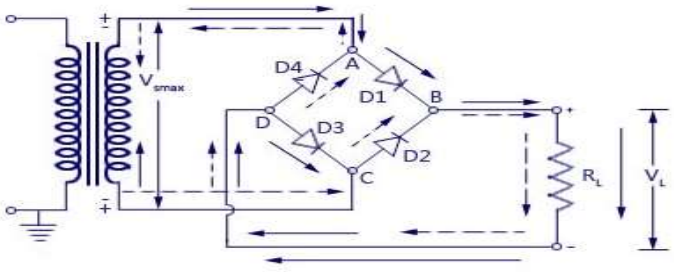
3A The filter capacitor C is placed across the resistance load RLoad.. The only difference is that two pulses of current will charge the capacitor during alternate positive (D1) and negative (D2) half cycles. Similarly capacitor C discharges twice through RLoad during one full cycle.

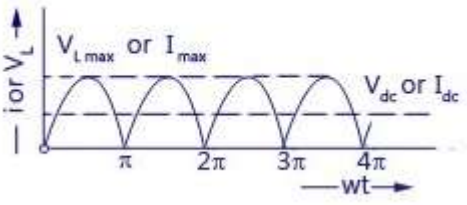


4A



Input Voltage Waveform





5A relaxation oscillator, square wave generator,comparator

6A inductive coupling,RC coupling,transformer coupling,direct coupling

7A Class A Amplifiers are the most common type of amplifier class due mainly to their simple design. Class A, literally means "the best class" of amplifier due mainly to their low signal distortion levels and are probably the best sounding of all the amplifier classes mentioned here. The class A amplifier has the highest linearity over the other amplifier classes and as such operates in the linear portion of the characteristics curve. Class B amplifiers were invented as a solution to the efficiency and heating problems associated with the previous class A amplifier. The basic class B amplifier uses two complimentary transistors either bipolar of FET for each half of the waveform with its output stage configured in a "push-pull" type arrangement, so that each transistor device amplifies only half of the output waveform.In the class B amplifier, there is no DC base bias current as its quiescent current is zero, so that the dc power is small and therefore its efficiency is much higher than that of the class A amplifier.

PART C

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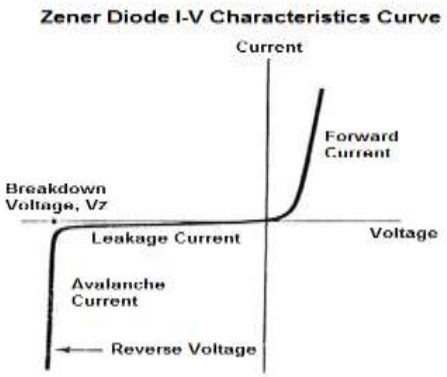
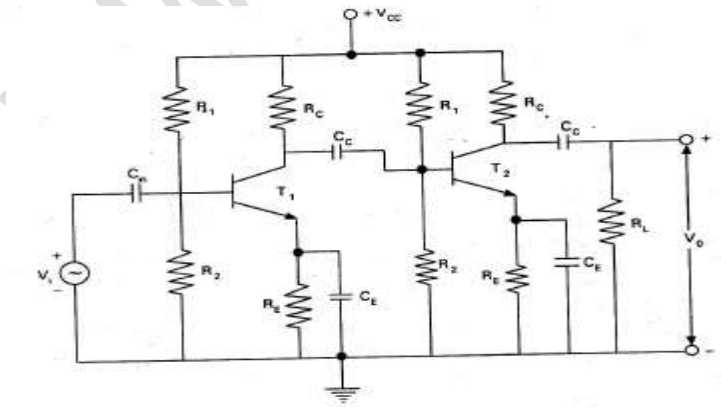
1A



Reverse characteristics of zener diode. Under reverse biasing condition , only a very small current will flows its due to minority charge carriers.If the reverse bias voltage is made too high, the current through the pn junction increases rapidly. This is called break down voltage. At this voltage the crystal structure will breaks down. There are 2 break downs.When reverse bias is increased the electric field at the junction also increase. High electric field causes covalent bond to break.so no.of carriers are generated. This causes large current to flow. This is called zener break down.The increased electric field causes increase in the velocities of minority carriers.These high energy carriers break covalent bonds,there by generating more carriers.again these generated carriers are accelerated by the electric field.A chain reaction is thus established.This is called avalanche break down**.**

(b) When an ac signal is applied to the input of first stage, it gets amplified by this stage and appears across the collector resistor itc of first-stage: This output voltage of first-stage is coupled to the base of the second stage through the coupling capacitor C. The amplified signal of first stage gets further amplification by the second stage and hence more amplification takes place. The output of the stage is taken out through the coupling the overall gain of amplification is equal so product of the individual stage gains. Av = Av1 * Av2 It Is to be noted that as the configuration employed Is CE configuration, each stage of amplification produces a phase shift of the input signal by 180. The overall phase shift is 2 x 180,or 360° or there's no phase difference between the input signal and the output of the second stage of amplification



IV (a) We know that, $I_E = I_C + I_B$ ... (1)

divide the above equation by I_C, we get

$$\frac{I_E}{I_C} = \frac{I_C}{I_C} + \frac{I_B}{I_C}$$

$$\frac{1}{\alpha} = 1 + \frac{1}{\beta}$$

$$\frac{1}{\beta} = \frac{1}{\alpha} - 1 = \frac{1-\alpha}{\alpha}$$

$$\therefore \quad \boxed{\beta = \frac{\alpha}{1-\alpha}} \qquad \text{... (2)}$$

from eq. (1), $I_B = I_E - I_C$

$$\therefore \quad \gamma = \frac{I_E}{I_B} = \frac{I_E}{I_E - I_C}$$

dividing the N.R and D.R on RHS by I_E, we get

$$\gamma = \frac{I_E/I_E}{\frac{I_E}{I_E} - \frac{I_C}{I_E}} = \frac{1}{1-\alpha}$$

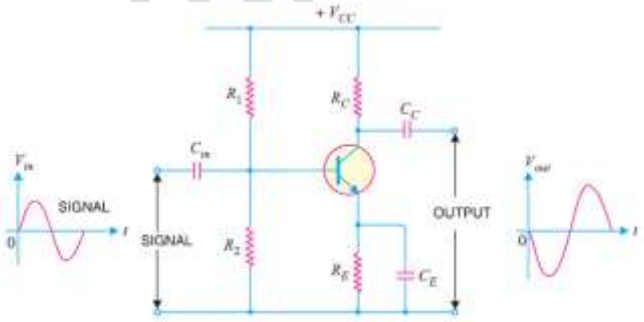
$$\therefore \quad \boxed{\gamma = \frac{1}{1-\alpha}}$$

Adding 1 to eq. (2) on both sides, we get

$$\beta + 1 = \frac{\alpha}{1-\alpha} + 1 = \frac{\alpha + 1 - \alpha}{1-\alpha} = \frac{1}{1-\alpha} = \gamma$$

$$\therefore \quad \gamma = \beta + 1.$$

(b)



The phase difference of 180° between the signal voltage and output voltage in a common emitter amplifier is known as phase reversal. Consider a common emitter amplifier circuit shown in Fig. The signal is fed at the input terminals and output is taken from collector and emitter end of supply. The total instantaneous output voltage is given by :

$$v_{CE} = V_{CC} - i_C R_C \qquad ...(i)$$

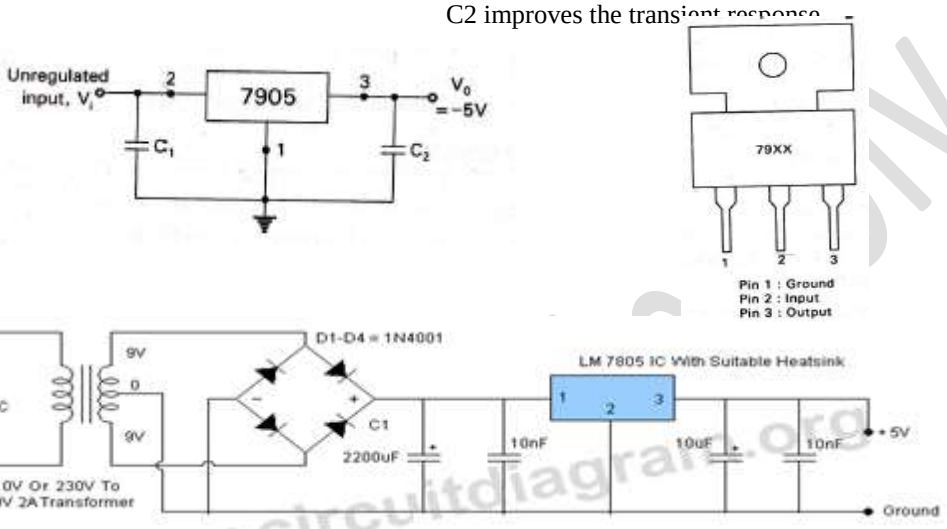
When the signal voltage increases in the positive half-cycle, the base current also increases. The result is that collector current and hence voltage drop icRc increases. As Vcc is constant, therefore, output voltage V decreases In other words, as the signal voltage is increasing in the positive half-cycle, the output voltage is increasing in the negative sense i.e. output is 180 out of phase with the input. It follows, therefore, that in a common emitter amplifier, the positive half-cycle of the signal appears as amplified negative half-cycle in the output and vice-versa The fact of phase reversal can be readily proved mathematically. Thus differentiating exp. (i), we get,

$$dv_{CE} = 0 - di_c R_C$$
$$dv_{CE} = -di_c R_C$$

V (a)

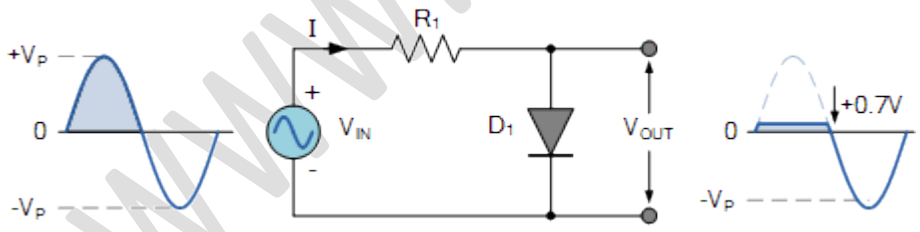
Characteristics	Half Wave Rectifier	Full Wave Rectifier
Definition	The Rectifier that converts only one half Cycle of the input AC supply to DC is called Half Wave Rectifier.	The Rectifier that converts both Halves of the AC input supply Cycle into DC is Called Full Wave Rectifier.
Diodes Used	One	Two/Four
Peak Inverse Voltage(PIV)	PIV=V_m	PIV=$2V_m$ (Centre Tap Rectifier) PIV=V_m (Bridge Rectifier)
DC Output Voltage	$V_{d.c.}=V_m/\pi=0.318Vm$	$V_{d.c.}=2V_m/\pi$
R.M.S. Current	$I_{rms}=I_m/2$	$I_{rms}=I^2_m/\sqrt{2}$
Ripple Factor	1.21	r= 0.48
Efficiency	40.6 %	81.2%

(b) pin 2 is the input terminal, pin 1 is the ground and pin 3 is the output terminal. The unregulated input voltage (V1) is given to the input terminal. The output is taken from the output terminal. Filter capacitors are shown to be connected at the input and output side. The input capacitor C1 is used to cancel the inductive effects due to long distiibution leads and the output capacitor C2 improves the transient response.



VI (a) A clipper is a device which limits, remove or prevents some portion of the wave form (input signal voltage) above or below a certain level

Positive Diode Clipping Circuits

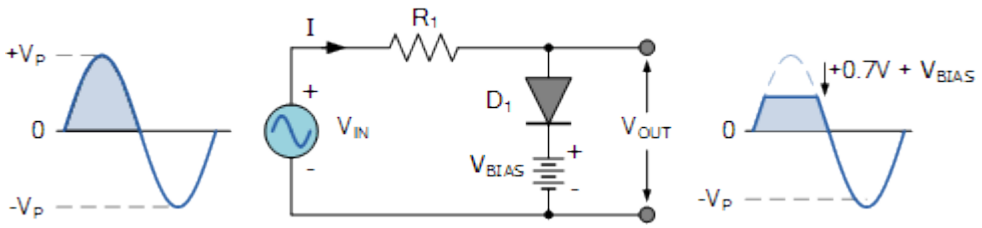


In this diode clipping circuit, the diode is forward biased (cathode more positive than anode) during the positive half cycle of the sinusoidal input waveform. For the diode to become forward biased, it must have the input voltage magnitude greater than +0.7 volts (0.3 volts for a germanium diode).

When this happens the diodes begins to conduct and holds the voltage across itself constant at 0.7V until the sinusoidal waveform falls below this value. Thus the output voltage which is taken across the diode can never exceed 0.7 volts during the positive half cycle.

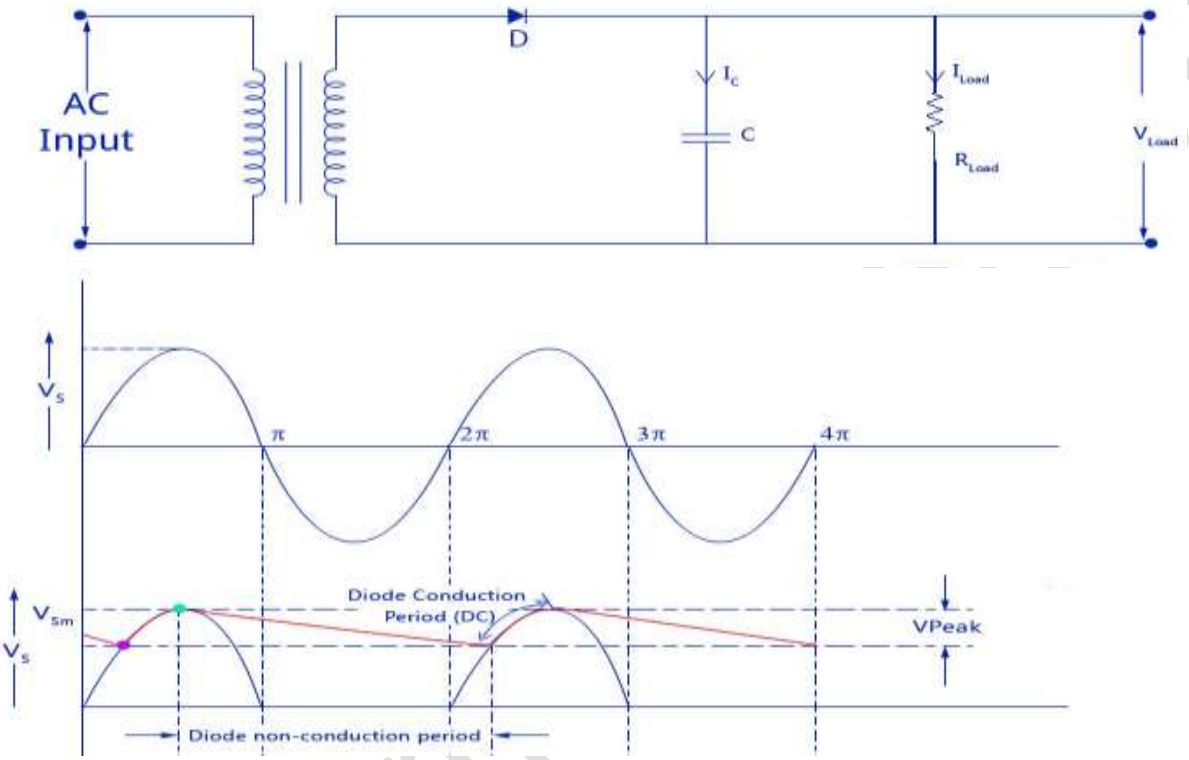
During the negative half cycle, the diode is reverse biased (anode more positive than cathode) blocking current flow through itself and as a result has no effect on the negative half of the sinusoidal voltage which passes to the load unaltered. Then the diode limits the positive half of the input waveform and is known as a positive clipper circuit.

Biased Diode Clipping Circuits



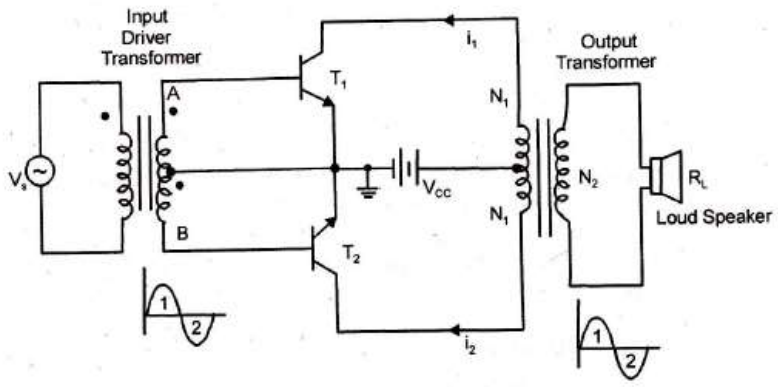
when a diode conducts the negative half cycle of the output waveform is held to a level $-V_{BIAS}$ - 0.7V

(b)



During the positive half cycle of the input ac voltage, the diode D will be forward biased and thus starts conducting. During this period, the capacitor 'C' starts charging to the maximum value of the supply voltage Vsm. When the capacitor is fully charged, it holds the charge until the input ac supply to the rectifier reaches the negative half cycle. As soon as the negative half supply is reached, the diode gets reverse biased and thus stops conducting. During the non-conducting period, the capacitor 'C' discharges all the stored charges through the output load resistance RLoad. As the voltage across RLoad and the voltage across the capacitor 'C' are the same (VLoad = Vc), they decrease exponentially with a time constant (C*RLoad) along the curve of the non-conducting period.

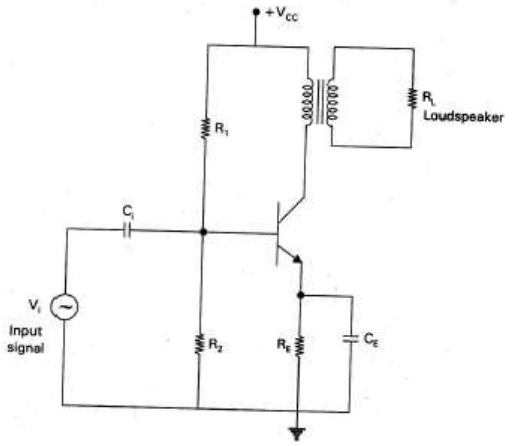
VII (a)

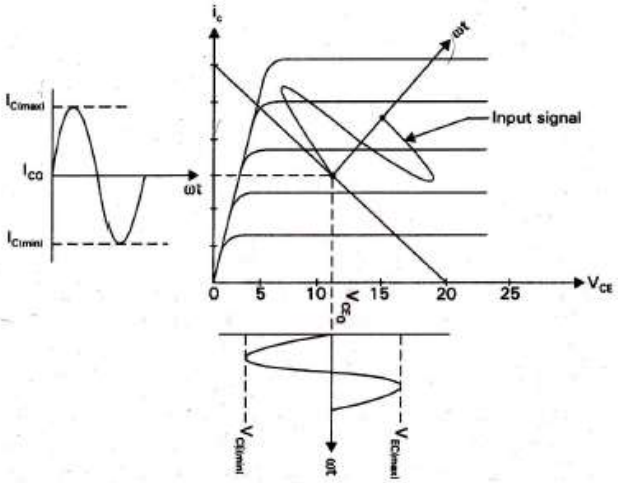


The input signal appears across the secondary AB of driver transformer. During the positive half cycle of the signal, end A becomes positive and end B negative. This will make the base - emitter junction of T, forward biased and that of T, reverse biased. The circuit will conduct current due to T, only, and is shown by current i,. Therefore, this half-cycle of the signal is amplified by T, and appears in the upper half of the primary of output transformer. During the negative half - cycle of the input signal, T2 is forward biased whereas T, is reverse biased. Therefore, T2 conducts and is shown by current i2. So, this half - cycle of the signal is amplified by T2 and appears in the lower half of the output transformer primary. The centre tapped primary of the output transformer combines two collector currents to form a sine wave output in the secondary. Thus the two transistors conduct in alternate half cycles of the input signal. Hence the collector current flow in opposite direction. So the net d.c in the primary is zero. However, the secondary of the output transformer will have induced voltage. Output of the amplifier will be twice that of the output offered by the single transistor. The push - pull arrangement also permits a maximum transfer of power to the load through impedance matching. The turns ratio 2 N, : N2 of the transformer is chosen so that the load R_L is matched with the output impedance of the transistor. If R_L is the resistance connected across the secondary of output transformer, then the resistance looking into the primary is

$$R_L^1 = \left(\frac{2N_1}{N_2}\right)^2 R_L$$

(b)



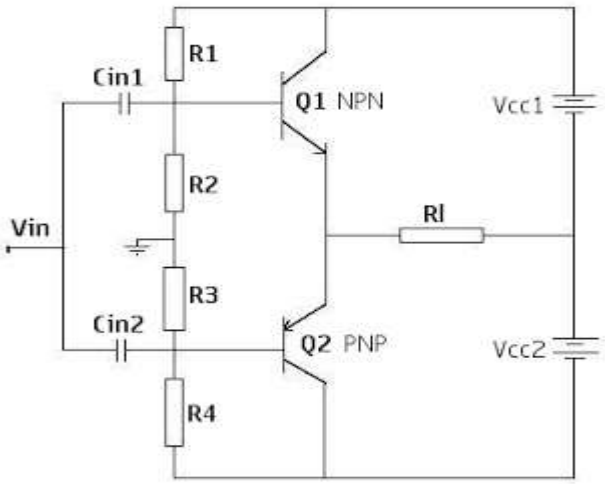


$$P_{0(ac)} = V_{CE\,(rms)} \times I_{C(rms)}$$

$$= \frac{V_{CE(Peak)}}{\sqrt{2}} \times \frac{I_{C(Peak)}}{\sqrt{2}}$$

It is also known as single-ended power amplifier (denoting only one transistor).The transistor is operated in class-A operating, the collector current flows for the complete cycle of the input signal. The circuit consists of an NPN transistor connected in CE configuration. Potential divider biasing is used with resistors RI, R2 and RE. The primary of the transformer is connected in series with the collector to the Vcc terminal. The load resistance (R_L is connected to the secondary of the transformer. Here, the transformer provides impedance matching. It match the loudspeaker resistance (i.e., R_L) to the output resistance of the amplifier, to achieve maximum possible power output.The operating point is so selected that the transistor works only in the linear portion of its characteristics. This enables the circuit to produce maximum equal positive and negative changes in V. The input signal varies the base current. This variation in base current and the corresponding variations in collector current and collertor voltage are shown. The variation of collector voltage appears across the primary of the transformer. An a.c. voltage is induced in the secondary, which in turn develops ac power in R_L. From the graph the maximum and minimum values of the collector current and voltage are noted. The ac power developed across the transformer primary can be calculated to be the same power across the $R_{L,}$ if the transformer is 100% efficient

VIII (a)



The signal applied at the input goes to the base of both the transistors. The two transistors conduct in the opposite half cycle of input signal, the NPN transistor Q1 is forward biased and conducts while the PNP transistor Q2 is reverse biased and so does not conduct. This results in a half cycle of output voltage across the load, resistor Rl. Similarly during the negative half cycle only the PNP transistor Q2 is forward biased and conducts which develops second half cycle of the output voltage across the Load Resistor Rl. Transistor Q1 being reverse biased and does not conduct during the negative half cycle of the input signal. Thus during a complete cycle of input, a complete cycle of output will developed.

(b) The F_L and F_H are lower and upper cut-off frequencies respectively, when frequency increases the capacitive reactance decreases so the capacitor will act as short to the coming signal and reduces the gain.

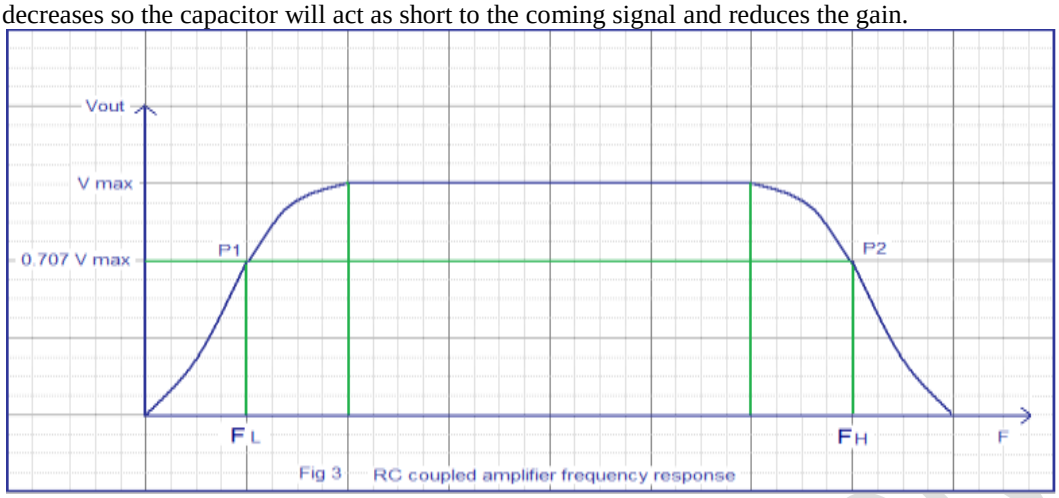


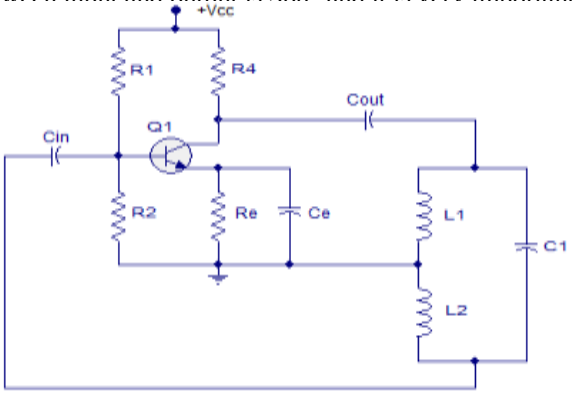
Fig 3 RC coupled amplifier frequency response

And also at high frequency there exists a capacitance called inter electrode capacitance. At low frequency the capacitive reactance is very high so the signal could not be properly coupled to the input of the transistor, so the gain will reduces. Between these the gain is found to be stable.

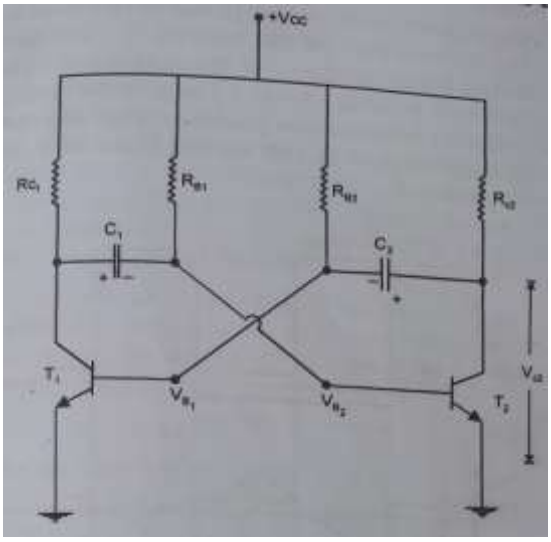
Bandwidth. The range of frequency that an amplifier can amplify properly is called the bandwidth Usually the bandwidth is measured based on the half power bandwidth is the difference between the lower and upper half power points. The band width of a good audio amplifier must be from 20 Hz to 20 KHz because that is the frequency range that is audible to the human ear. The frequency response of a single stage RC coupled transistor is shown in the figure Points tagged P1 and P2 are the lower and upper half power points respectively.

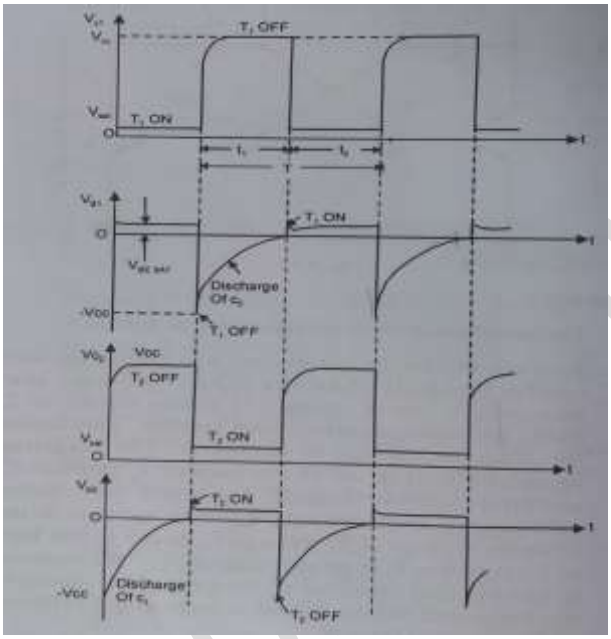
Gain. Gain of an amplifier is the ratio of output power to the input power. It represents how much an amplifier can amplify a given signal. Gain can be simply expressed in numbers or in decibel (dB). Gain in number is expressed by the equation G = P*out* / *Pin*. In decibel the gain is expressed by the equation Gain in dB = 10 log (P*out* / P*in*). Here Pout is the power output and Pin is the power input. Gain can be also expressed in terms of output voltage / input voltage or output current / input current. Voltage gain in decibel can be expressed using the equation, Av in dB = 20 log (V*out* / V*in*) and current gain in dB can be expressed using the equation Ai = 20 log (I*out* / I*in*

IX (a) Resistors R1 and R2 give a potential divider bias for the transistor Q1. Re is the emitter resistor, whose job is to provide thermal stability for the transistor. Ce is the emitter by pass capacitors, which by-passes the amplified AC signals. If the emitter by-pass capacitor not there, the amplified ac voltages will drop across Re and it will get added on to the base-emitter voltage of Q1 and will disrupt the biasing conditions. Cin is the input DC decoupling capacitor while Cout is the output DC decoupling capacitor. The task of a DC decoupling capacitor is to prevent DC voltages from reaching the succeeding stage. Inductor L1, L2 and capacitor C1 forms the tank circuit.When the power supply is switched ON the transistor starts conducting and the collector current increases. As a result the capcitor C1 starts charging and when the capacitor C1 is fully charged it starts discharging through coil L1. This charging and discharging creates a series of damped oscillations in the tank circuit and it is the key.The oscillations produced in the tank circuit is coupled (fed back) to the base of Q1 and it appears in the amplified form across the collector and emitter of the transistor. The output voltage of the transistor (voltage across collector and emitter) will be in phase with the voltage across inductor L1. Since the junction of two inductors is grounded, the voltage across L2 will be 180° out of phase to that of the voltage across L1. The voltage across L2 is actually fed back to the base of Q1. From this we can see that, the feed back voltage is 180° out of phase with the transistor and also the transistor itself will create another 180° phase difference. So the total phase difference between input and output is 360° and it is very important condition for creating sustained oscillations.



(b) Because of circuit variations, one transistor will conduct heavily than the other. Assume that transistor T1 starts conducting before. transistor T2 does. Its collector current rises rapidly. This causes its collector voltage to decrease. The resulting negative signal is fed to the base of T2 through C1 and drives it towards cutoff. As a result, the collector voltage of T2 rises towards Vcc. The increase in the collector voltage of T2 through C2 is fed to the base of T1 . It causes T1 to go into saturation. This happens SO quickly that capacitor C1 does not get a chance to discharge and the decreased voltage at the collector of T1 appears across RB1





The off time for transistor T_2 is t_2

$$t_2 = 0.693\ R_{B1}\ C_1$$

The off time for transistor T_1 is t_1

$$t_1 = 0.693\ R_{B2}\ C_2$$

$\therefore$ Total period, $T = t_1 + t_2 = 0.693\ (R_{B1}\ C_1 + R_{B2}\ C_2)$

For a symmetric circuit with $R_{B1} = R_{B2} = R$ and $C_1 = C_2 = C$, we have

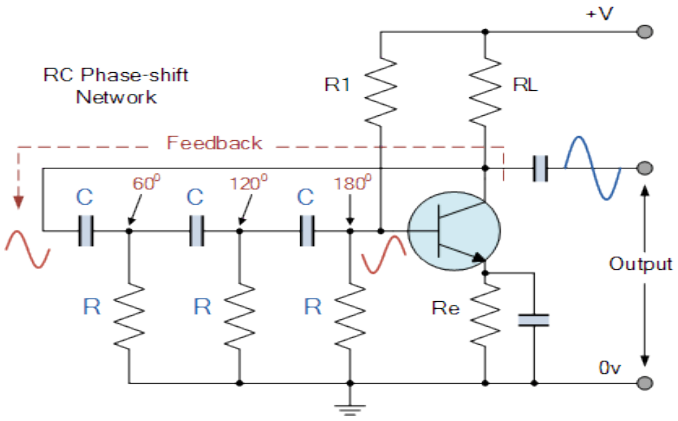
$$T = 1.386\ RC, \text{ seconds.}$$

and

$$f = \frac{1}{T} = \frac{1}{1.386\,RC}\ \text{Hz.}$$

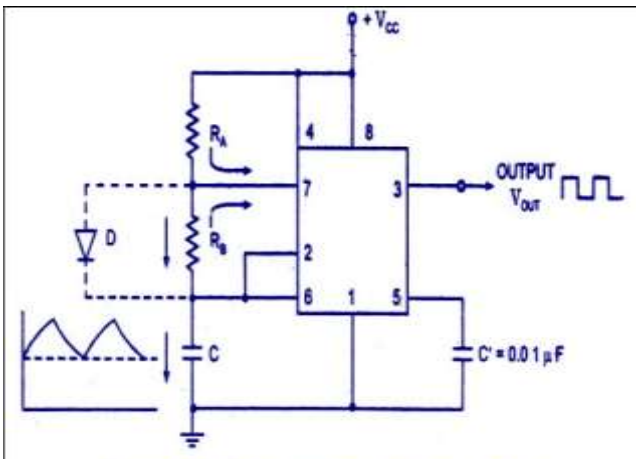
X(a) The basic **RC Oscillator** which is also known as a **Phase-shift Oscillator**, produces a sine wave output signal using regenerative feedback obtained from the resistor-capacitor combination. This regenerative feedback from the RC network is due to the ability of the capacitor to store an electric charge, (similar to the LC tank circuit).This resistor-capacitor feedback network can be connected as shown above to produce a leading phase shift (phase advance network) or interchanged to produce a lagging phase shift (phase retard network) the outcome is still the same as the sine wave oscillations only occur at the frequency at which the overall phase-shift is 360°.By varying one or more of the resistors or capacitors in the phase-shift network, the frequency can be varied and generally this is done by keeping the resistors the same and using a 3-ganged variable capacitor.If all the resistors, R and the capacitors, C in the phase shift network are equal in value, then the frequency of oscillations produced by the RC oscillator is given as:

$$f_r = \frac{1}{2\pi RC\sqrt{2N}}$$

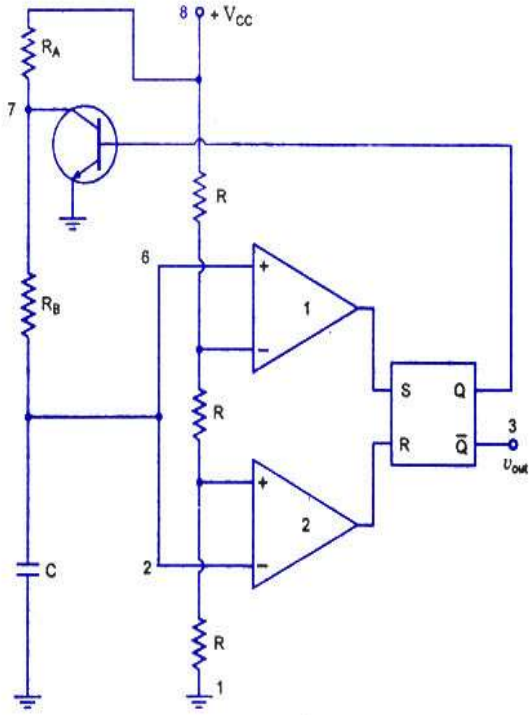


If a three-stage RC phase-shift network is connected between this input and output of the amplifier, the total phase shift necessary for regenerative feedback will become 3 x 60^o + 180^o = 360^o

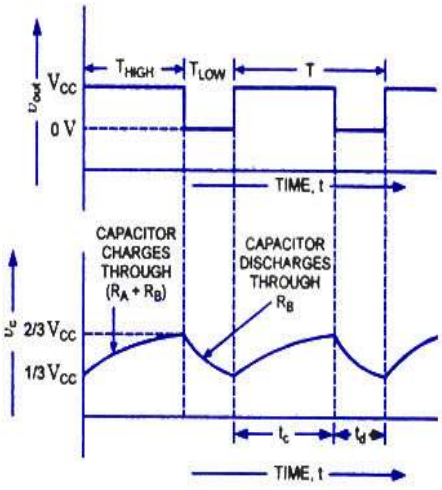
(b) when Q is low or output V_{OUT} is high, the discharging transistor is cut-off and the capacitor C begins charging toward V_{CC} through resistances R_A and R_B. Because of this, the charging time constant is (R_A + R_B) C. Eventually, the threshold voltage exceeds +2/3 V_{CC}, the comparator 1 has a high output and triggers the flip-flop so that its Q is high and the timer output is low. With Q high, the discharge transistor saturates and pin 7 grounds so that the capacitor C discharges through resistance R_B with a discharging time constant R_B C. With the discharging of capacitor, trigger voltage at inverting input of comparator 2 decreases. When it drops below 1/3V_{CC}, the output of comparator 2 goes high and this reset the flip-flop so that Q is low and the timer output is high. This proves the auto-transition in output from low to high and then to low as, illustrated in fig ures. Thus the cycle repeats.



Circuit of The Timer 555 as an Astable Multivibrator



Internal Circuitry With External Connections



Capacitor and Output Voltage Waveforms

Astable Operation