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THIRD SEMESTER DIPLOMA EXAMINATION IN ELECTRICAL & ELECTRONICS ENGINEERING, MARCH 2012

ELECTRONIC DEVICES AND CIRCUITS

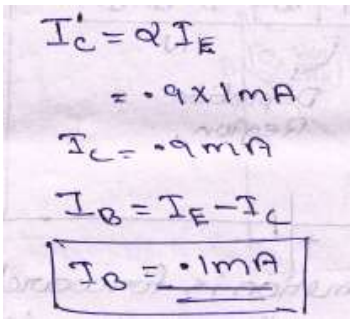
Time :3hours Maximum marks:100

PART A (maximum marks 10)

I. Answer the following questions in 2 or 3 sentences: marks

1A. It is the ratio of output AC to output DC

2A




3A it is used to filter the ac components from the rectifiers.

4A it increases the gain of the amplifier. It increases the net i/p to the amplifier.

5A Circuit which produces electrical oscillations of any desired frequency is called tank circuit

PART B (Maximum marks :30)

II Answer any five questions from the following

1A **FORWARD BIASED PN JUNCTION:**The holes are repelled from the +ve terminal of the battery and are compelled to move towards the junction. Electrons repel led from –ve terminal of the battery and drift towards the junction. Due to its energy some electrons and holes will penetrate the depletion region. This reduces the potential barrier. Majority carriers diffuse across the junction. These carriers recombine and cause movement of charge carriers in the space charge region. For each recombination of free electron and hole that occurs, an electron from the –ve terminal of battery enters the N type material. It then drift towards the junction.The flow of carriers due to applied voltage is called drift current and whereas the current flows as a result of gradient of carrier concentration is called diffusion current.

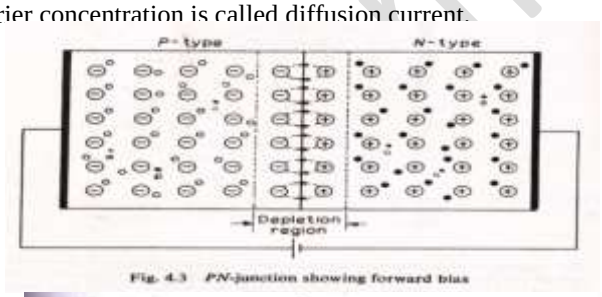


Fig. 4.3 *PN*-junction showing forward bias

2A .

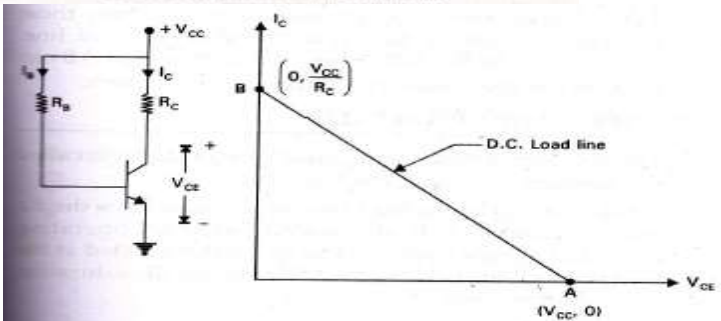


Fig. 1.30 Fig. 1.31 DC Load Line

The values of $V_{CC}$ and $R_C$ are fixed and $I_C$ and $V_{CE}$ are dependent on $R_B$.

Applying KVL to the collector circuit, we get

$$V_{CC} = I_C R_C + V_{CE} \quad \ldots (1)$$

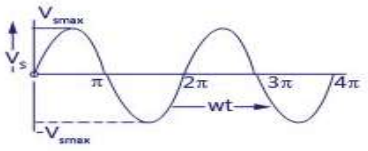
(or) $$I_C = -\frac{1}{R_C} V_{CE} + \frac{V_{CC}}{R_C} \quad \ldots (2)$$

(i) If $I_C = 0$, then $V_{CE} = V_{CC}$
This gives the point, A = $(V_{CC}, 0)$
At point A, the transistor is in cut off condition.

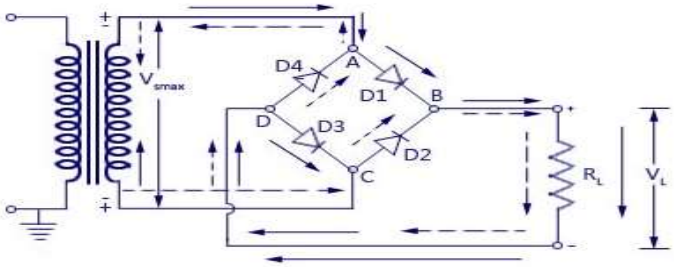
(ii) If $V_{CE} = 0$, then $I_C = \frac{V_{CC}}{R_C}$

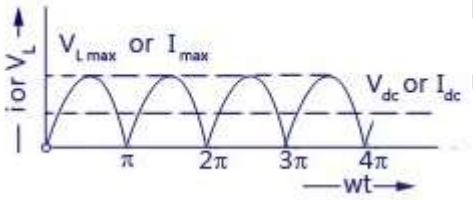
This gives the point, B = $\left(0, \frac{V_{CC}}{R_C}\right)$.

3A



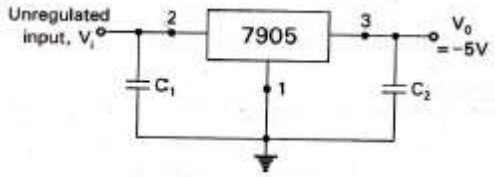

Input Voltage Waveform

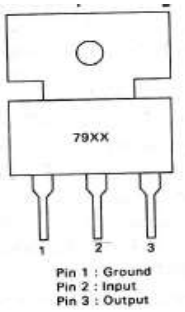


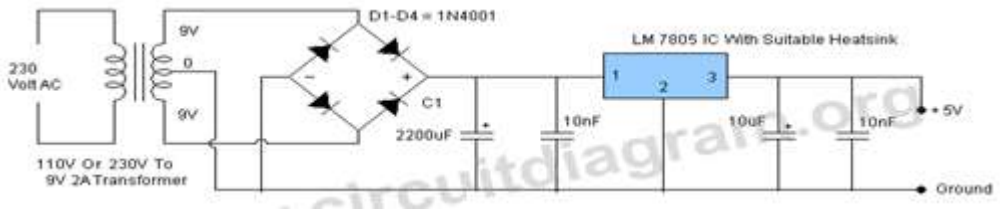

During first half cycle of the input voltage, the upper end of the transformer secondary winding is positive with respect to the lower end. Thus during the first half cycle diodes D1 and $D_3$ are forward biased and current flows through arm AB, enters the load resistance $R_L$, and returns back flowing through arm DC. During this half of each input cycle, the diodes $D_2$ and $D_4$ are reverse biased and current is not allowed to flow in arms AD and BC. The flow of current is indicated by solid arrows in the figure above. We have developed another diagram below to help you understand the current flow quickly. During second half cycle of the input voltage, the lower end of the transformer secondary winding is positive with respect to the upper end. Thus diodes $D_2$ and $D_4$ become forward biased and current flows through arm CB, enters the load resistance $R_L$, and returns back to the source flowing through arm DA. Flow of current has been shown by dotted arrows in the figure. Thus the direction of flow of current through the load resistance $R_L$ remains the same during both half cycles of the input supply voltage

4A



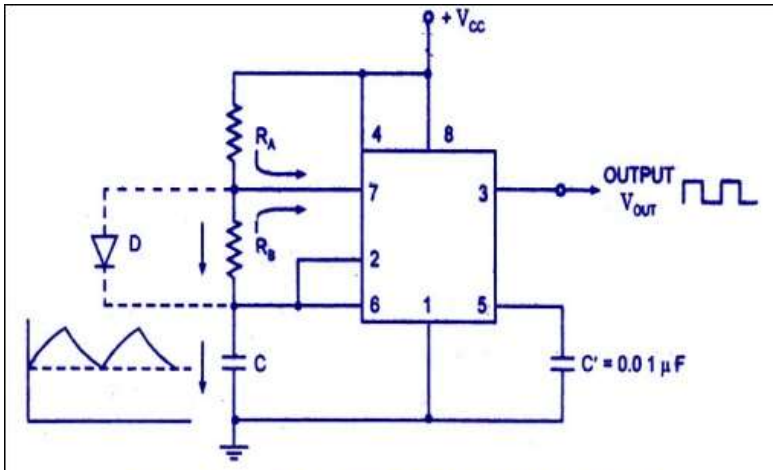

pin 2 is the input terminal, pin 1 is the ground and pin 3 is the output terminal. The unregulated input voltage (V1) is given to the input terminal. The output is taken from the output terminal. Filter capacitors are shown to be connected at the input and output side. The input capacitor C1 is used to cancel the inductive effects due to long distiibution leads and the output capacitor C2 improves the transient response.




5A Bandwidth can be defined as range of frequencies over which the gain is equal to or greater than 0.707 .the frequencies at which the voltage gain reduces to 0.707 of the maximum gain are known as cut off frequencies of the amplifier.

6A Improves the stability of gain, increases the i/p impedence, increases band width, it decreases the o/p impedance, It reduces the distortion and noise.

7A




*Circuit of The Timer 555 as an Astable Multivibrator*

**PART C**

**111**

(a) We know that, $I_E = I_C + I_B$ ... (1)

divide the above equation by $I_C$, we get

$$\frac{I_E}{I_C} = \frac{I_C}{I_C} + \frac{I_B}{I_C}$$

$$\frac{1}{\alpha} = 1 + \frac{1}{\beta}$$

$$\frac{1}{\beta} = \frac{1}{\alpha} - 1 = \frac{1-\alpha}{\alpha}$$

$$\therefore \quad \boxed{\beta = \frac{\alpha}{1-\alpha}} \qquad \text{... (2)}$$

from eq. (1), $I_B = I_E - I_C$

$$\therefore \quad \gamma = \frac{I_E}{I_B} = \frac{I_E}{I_E - I_C}$$

dividing the N.R and D.R on RHS by $I_E$, we get

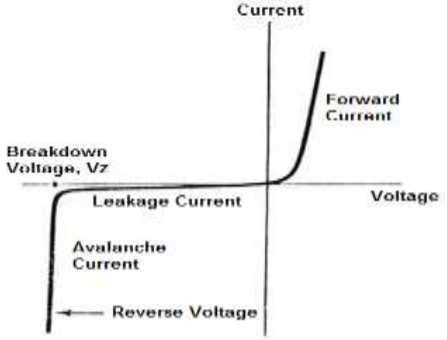
$$\gamma = \frac{I_E/I_E}{\frac{I_E}{I_E} - \frac{I_C}{I_E}} = \frac{1}{1-\alpha}$$

$$\therefore \quad \boxed{\gamma = \frac{1}{1-\alpha}}$$

Adding 1 to eq. (2) on both sides, we get

(b) $$\beta + 1 = \frac{\alpha}{1-\alpha} + 1 = \frac{\alpha + 1 - \alpha}{1-\alpha} = \frac{1}{1-\alpha} = \gamma$$

Zener Diode I-V Characteristics Curve



**Reverse characteristics of zener diode:** Under reverse biasing condition , only a very small current will flows its due to minority charge carriers.If the reverse bias voltage is made too high, the current through the pn junction increases rapidly. This is called break down voltage. At this voltage the crystal structure will breaks down. There are 2 break downs.When reverse bias is increased the electric field at the junction also increase. High electric field causes covalent bond to break.so no.of carriers are generated. This causes large current to flow. This is called zener break down.The increased electric field causes increase in the velocities of minority carriers.These high energy carriers break covalent bonds,there by generating more carriers.again these generated carriers are accelerated by the electric field.A chain reaction is thus established.This is called avalanche break down**.**

IV (a) **Common emitter configuration and its Input characteristics:**

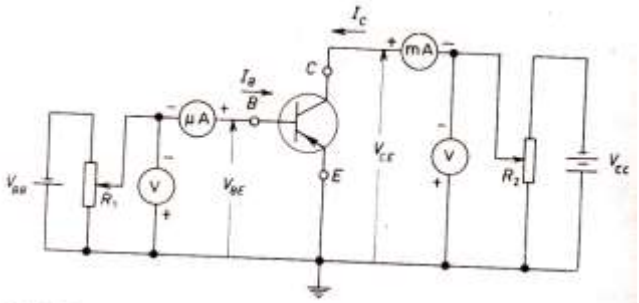



Fig. 5.17 Circuit arrangements for determining the static characteristics of a *PNP* transistor, in CE configuration

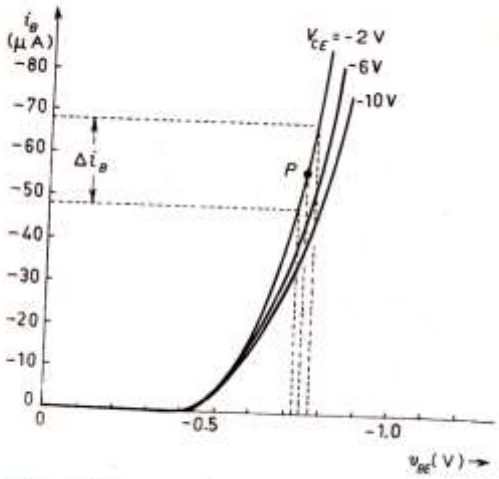



Fig. 5.18 Common-emitter input characteristics of a *PNP* transistor

It is plotted between Vbe and Ib ,making Vce constant..The base emitter junction is forward biased,when the Vce increases the curve resembles like a diode.

$$r_i = \left.\frac{\Delta V_{BE}}{\Delta I_B}\right|_{V_{CE}=\text{constant}}$$

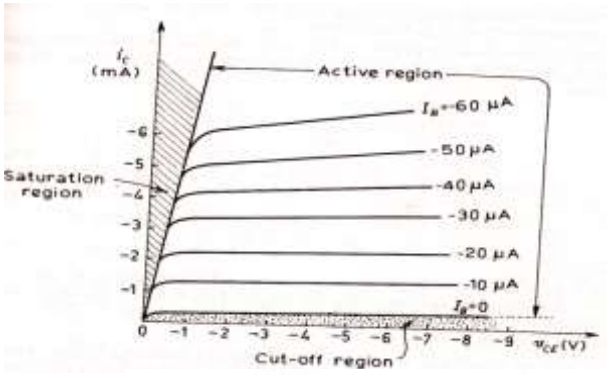
**Output CE characteristics**

**.** In active region,Ic slowly increases as Vce increases.

**.** Ic decreases rapidly when Vce decreases.At this condition the collector base junction is in forward biased .this is called saturation region

**.** In active region,the Ic is beta times greater than the Ib.so for small i/p current ,the Ib produces a large o/p current Ic.

**.**The Ic will not be zero when Ib is zero,there exists a small leakage current called Iceo




(a)

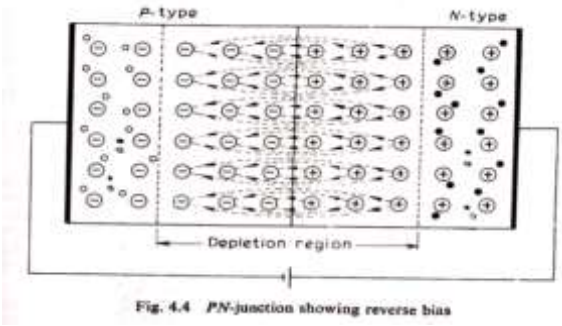
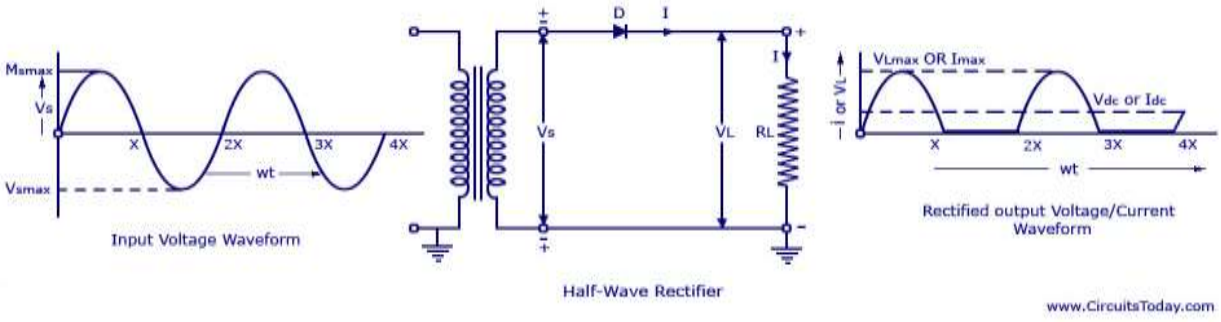


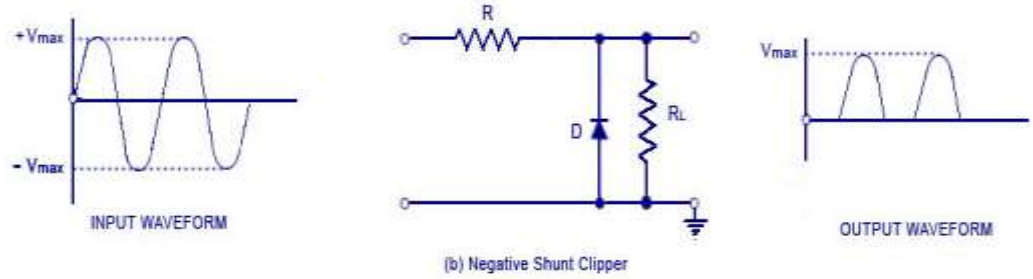

Fig. 4.4 *PN*-junction showing reverse bias

In p type the majority charge carriers are holes and in N type it is electrons.The p type semiconductor is attached to a negative terminal of the battery and n type semiconductor is attached to a positive terminal of the battery. if a reverse biasing potential is applied across these semiconductors then the holes and electrons are attracted to the terminal there by increasing the depletion region width. So the majority charge carriers will move away from the junction, hence the minority charge carriers will cause a small current while crossing the junction.

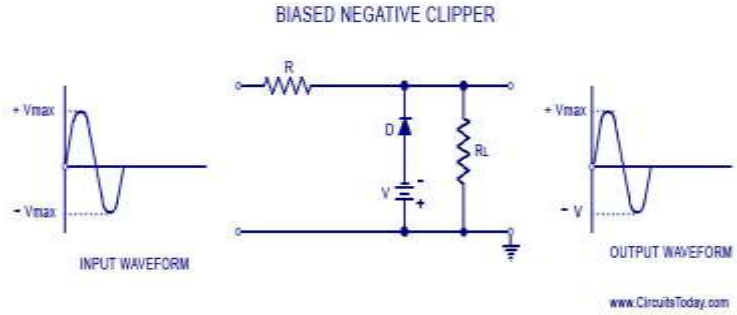
**V (a)** The input we give here is an alternating current. This input voltage is stepped down using a transformer. The reduced voltage is fed to the diode 'D' and load resistance RL. During the positive half cycles of the input wave, the diode 'D' will be forward biased and during the negative half cycles of input wave, the diode 'D' will be reverse biased. We take the output across load resistor RL. Since the diode passes current only during one half cycle of the input wave, we get an output as shown in diagram. The output is positive and significant during the positive half cycles of input wave. At the same time output is zero or insignificant during negative half cycles of input wave. This is called **half wave rectification**




(b) The negative clipping circuit is almost same as the positive clipping circuit, with only one difference. If the diode figures is reconnected with reversed polarity, the circuits will become for negative shunt clipper respectively.




When a small portion of the negative half cycle is to be removed, it is called a biased negative clipper.

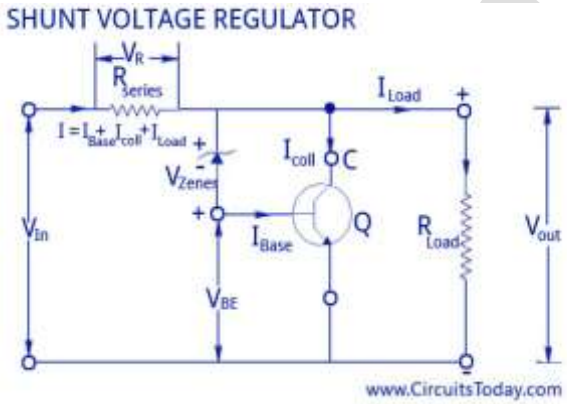



when the input signal voltage is positive, the diode 'D' is reverse-biased. This causes it to act as an open-switch. Thus the entire positive half cycle appears across the load, as illustrated by output waveform [figure (a)]. When the input signal voltage is negative but does not exceed battery the voltage 'V', the diode 'D' remains reverse-biased and most of the input voltage appears across the output. When during the negative half cycle of input signal, the signal voltage becomes more than the battery voltage V, the diode D is forward biased and so conducts heavily. The output voltage is equal to '- V' and stays at '- V' as long as the magnitude of the input signal voltage is greater than the magnitude of the battery voltage, 'V'. Thus a biased negative clipper removes input voltage when the input signal voltage becomes greater than the battery voltage.

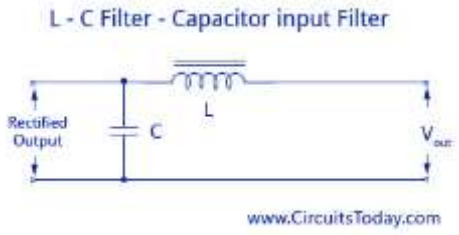
V1 (a) As there is a voltage drop in the series resistance Rseries the unregulated voltage is also decreased along with it. The amount of voltage drop depends on the current supplied to the load Rload.

Vout = Vzener + Vbe = Vin – I.Rseries

When the supply voltage increases, the output voltage and base emitter voltage of transistor increases and thus increases the base current Ibase and therefore causes an increase in the collector current Icoll (Icoll = β.Ibase).Thus, the supply voltage increases causing an increase in supply current, which inturn causes a voltage drop i the series resistance Rseries and thereby decreasing the output voltage. This decrease will be more than enough to compensate for the initial increase in output voltage. Thus, the output remains nearly a constant. The working explained above happens in reverse if the supply voltage decreases.When the load resistance Rload decreases, the load current Iload increases due to the decrease in currents through base and collector Ibase and Icoll. Thus, there will not be any voltage drop across Rseries and the input current remains constant. Thus, the output voltage will remain constant and will be the difference of the supply voltage and the voltage drop in the series resistance. It happens in reverse if there is an increase in load resistance.

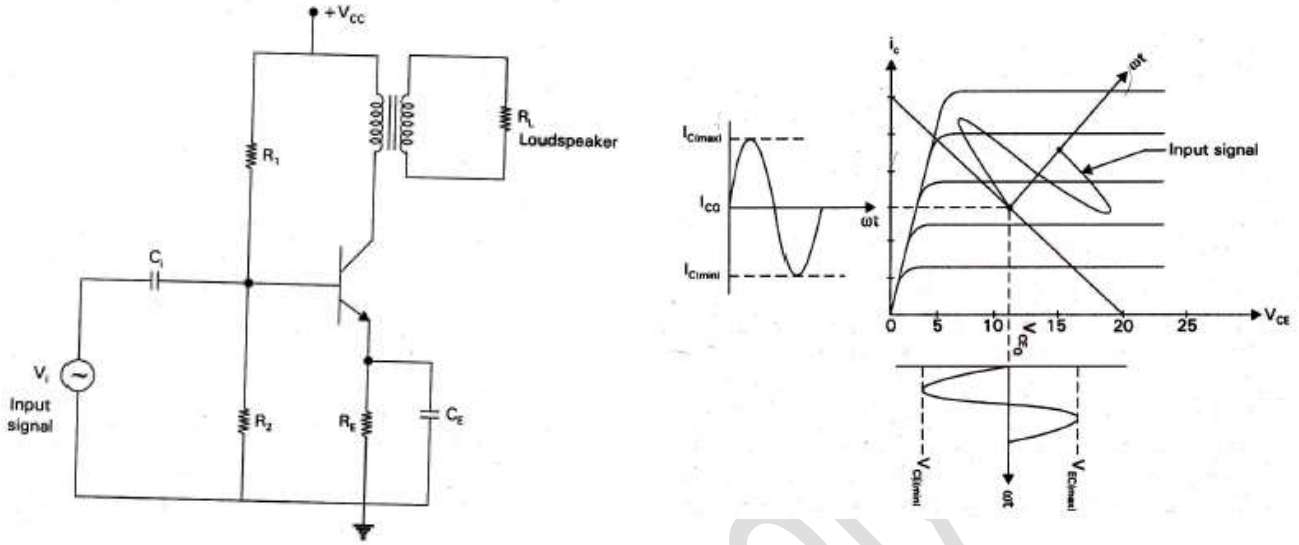



(a) The name pi – Filter implies to the resemblance of the circuit to a Π shape with two shunt capacitances (C1 and C2) and an inductance filter 'L'. As the rectifier output is provided directly into the capacitor it also called a capacitor input filter.The output from the rectifier is first given to the shunt capacitor C. The rectifier used can be half or full wave and the capacitors are usually electrolytic even though they large in size. In practical applications, the two capacitances are enclosed in a metal container which acts as a common ground for the two capacitors.



The Π – Filter has some advantages like higher dc voltage and smaller ripple factor. But it also has some disadvantages like poor voltage regulation, high peak diode current, and high peak inverse voltage.This filter is divided into two – a capacitor filter and a L-section filter. The capacitor C1 does most of the filtering in the circuit and the remaining ripple os removed by the L-section filter (L-C2). C1 is selected to provide very low reactance to the ripple frequency. The voltage regulation is poor for this circuit as the output voltage falls off rapidly with the increase in load current.

V11 (a)

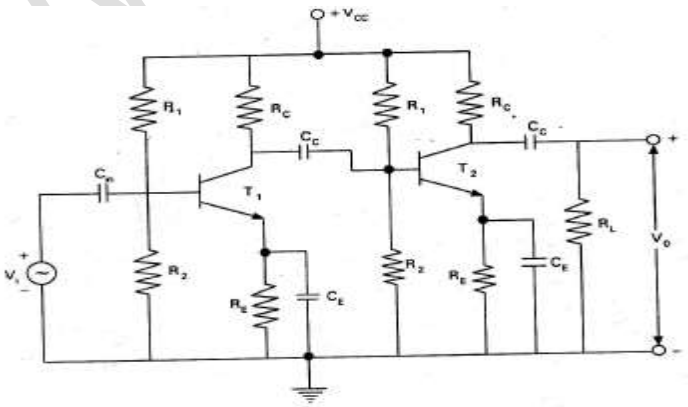



$$P_{0(ac)} = V_{CE\,(rms)} \times I_{C(rms)}$$

$$= \frac{V_{CE(Peak)}}{\sqrt{2}} \times \frac{I_{C(Peak)}}{\sqrt{2}}$$

It is also known as single-ended power amplifier (denoting only one transistor).The transistor is operated in class-A operating, the collector current flows for the complete cycle of the input signal. The circuit consists of an NPN transistor connected in CE configuration. Potential divider biasing is used with resistors RI, R2 and RE. The primary of the transformer is connected in series with the collector to the Vcc terminal. The load resistance ($R_L$ is connected to the secondary of the transformer. Here, the transformer provides impedance matching. It match the loudspeaker resistance (i.e., $R_L$) to the output resistance of the amplifier, to achieve maximum possible power output.The operating point is so selected that the transistor works only in the linear portion of its characteristics. This enables the circuit to produce maximum equal positive and negative changes in V. The input signal varies the base current. This variation in base current and the corresponding variations in collector current and collertor voltage are shown. The variation of collector voltage appears across the primary of the transformer. An a.c. voltage is induced in the secondary, which in turn develops ac power in $R_L$. From the graph the maximum and minimum values of the collector current and voltage are noted. The ac power developed across the transformer primary can be calculated to be the same power across the $R_{L,}$ if the transformer is 100% efficient

(b)

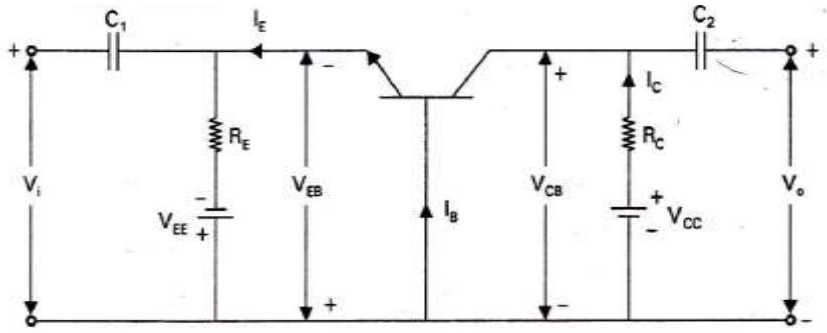



When an ac signal is applied to the input of first stage, it gets amplified by this stage and appears across the collector resistor itc of first-stage: This output voltage of first-stage is coupled to the base of the second stage through the coupling capacitor C. The amplified signal of first stage gets further amplification by the second stage and hence more amplification takes place. The output of the stage is taken out through the coupling the overall gain of amplification is equal so product of the individual stage gains. Av = Av1 * Av2 It Is to be noted that as the configuration employed Is CE configuration, each stage of amplification produces a

phase shift of the input signal by 180. The overall phase shift is 2 x 180,or 360° or there's no phase difference between the input signal and the output of the second stage of amplification

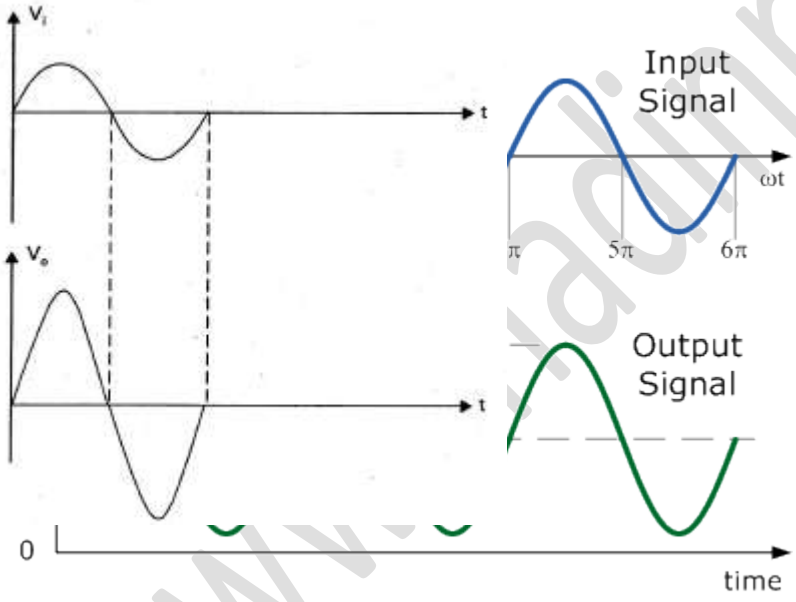
V111

(a)

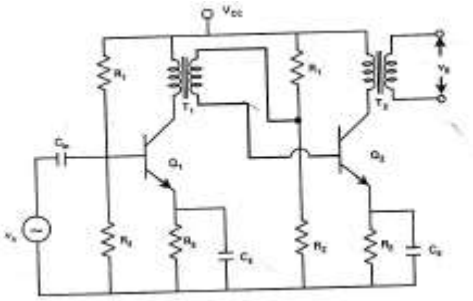



$$V_0 = V_{CC} - I_C R_C$$

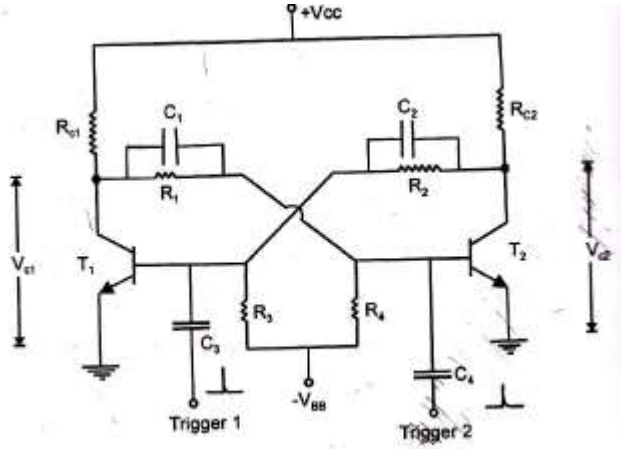
The emitter base junction is forward biased by power supply VEE, and the collector-base junction is reverse biased by Vcc. So, the transistor remains in the active region throughout its operation. C1 and C2 are coupling capacitors to provide d.c. isolation at the input and output of the amplifier. When a sinusoidal a.c. signal is applied at the input, during the positive half cycle of the applied signal, the amount of forward bias to base-emitter junction is decreased, resulting in a decrease in Is and hence Ic also decreases. The drop lc Rc decreases, hence Vs Vco correspondingly increases. Thus, a positive-going input signal produces a positive-going output signal, there is no phase reversal between the two. During the negative half cycle of the input signal, the forward bias to emitter-base junction is increased, resulting in a increase in Ie and hence lc also increases. So, the drop lc Rc

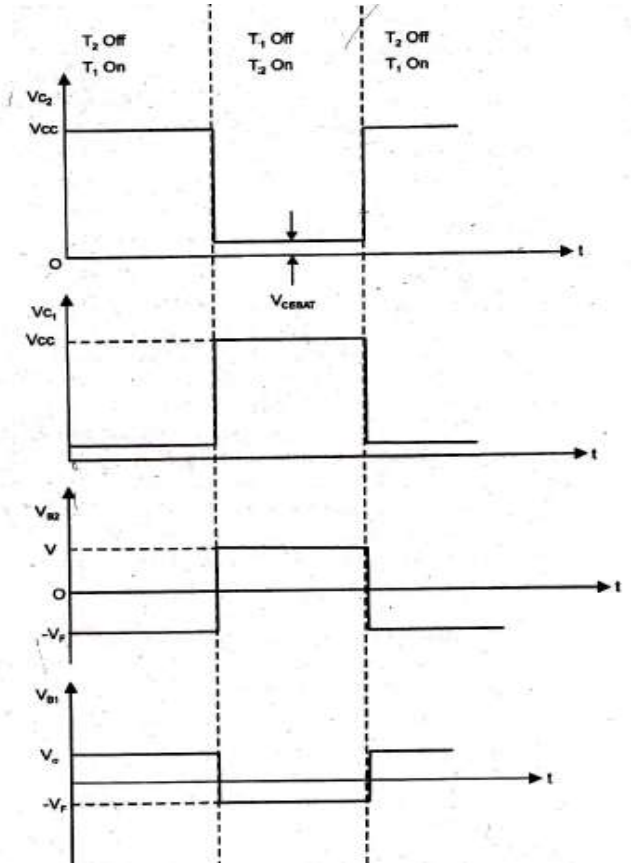



(b) The input ac signal is applied to the base of the first stage transistor. It is amplified by the first stage and appears across the primary winding of the transformer T,. The amplified ac voltage across the primary winding of T, is transferred to the secondary winding,by induction and is given to the input of the second stage. It ls further amplified by the second stage amplifier. The output appears across the secondary winding of transformer, T2

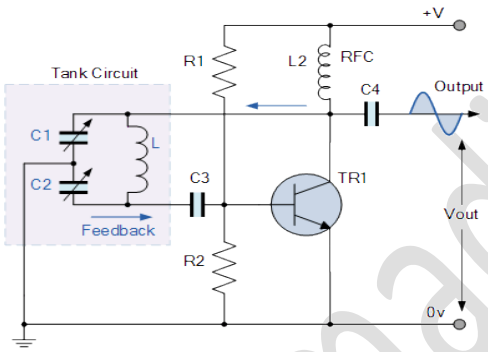
Application  ing signals.it is used in power amplifiers

1X (a) When $V_{cc}$ is applied, one transistor will start conducting slightly ahead of the other due to some differences in the characteristics of the transistors. Assume that T1 is turned ON and T2 is cutoff. The circuit will stay in this stable state until a trigger pulse is applied. Now, a positive trigger pulse of sufficient amplitude is applied to the base of T2 through C4. It will cause T2 to conduct. This will reduce the forward bias on T1 and cause a decrease in its collector current and an increase in collector voltage. The rising collector voltage is coupled to the base of T2 where it forward biases the base-emitter junction of T2. With this set of actions taking place, T2 is quickly drive to saturation and T1 to cutoff. The circuit will now remain stable in this state until a positive trigger pulse at T1 changes this state.



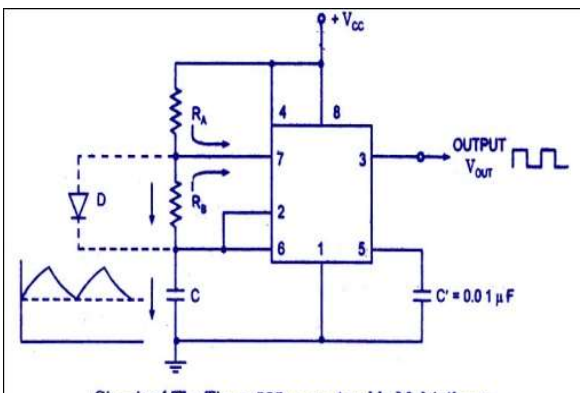




(b)

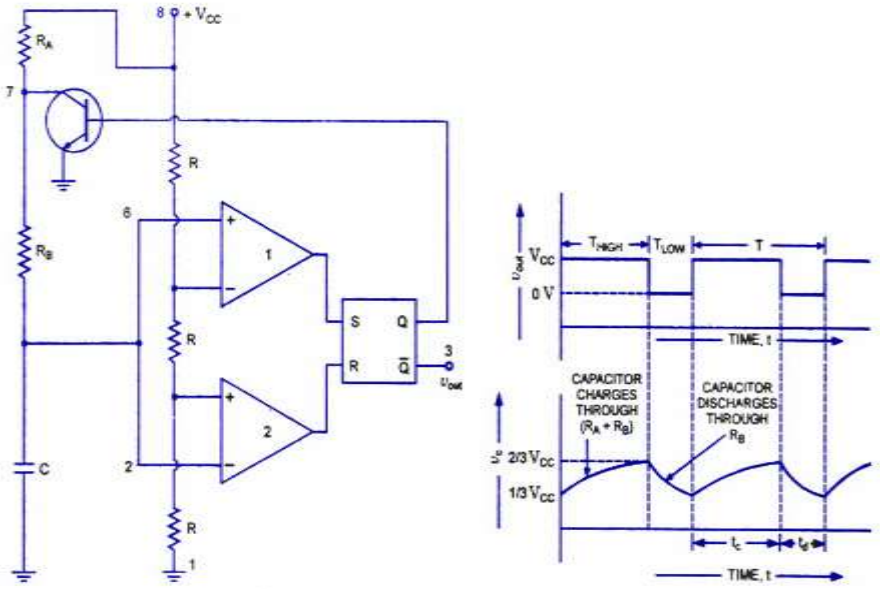



The transistor amplifiers emitter is connected to the junction of capacitors, C1 and C2 which are connected in series and act as a simple voltage divider. When the power supply is firstly applied, capacitors C1 and C2 charge up and then discharge through the coil L. The oscillations across the capacitors are applied to the base-emitter junction and appear in the amplified at the collector output.The amount of feedback depends on the values of C1 and C2 with the smaller the values of C the greater will be the feedback.The required external phase shift is obtained in a similar manner to that in the Hartley oscillator circuit with the required positive feedback obtained for sustained un-damped oscillations. The amount of feedback is determined by the ratio of C1 and C2. These two capacitances are generally "ganged" together to provide a constant amount of feedback so that as one is adjusted the other automatically follows.

X (a) when Q is low or output $V_{OUT}$ is high, the discharging transistor is cut-off and the capacitor C begins charging toward $V_{CC}$ through resistances $R_A$ and $R_B$. Because of this, the charging time constant is $(R_A + R_B)$ C. Eventually, the threshold voltage exceeds +2/3 $V_{CC}$, the comparator 1 has a high output and triggers the flip-flop so that its Q is high and the timer output is low. With Q high, the discharge transistor saturates and pin 7 grounds so that the capacitor C discharges through resistance $R_B$ with a discharging time constant $R_B$ C. With the discharging of capacitor, trigger voltage at inverting input of comparator 2 decreases. When it drops below 1/3$V_{CC}$, the output of comparator 2 goes high and this reset the flip-flop so that Q is low and the timer output is high. This proves the auto-transition in output from low to high and then to low as, illustrated in fig ures. Thus the cycle repeats.




*Circuit of The Timer 555 as an Astable Multivibrator*




*Internal Circuitry With External Connections* *Capacitor and Output Voltage Waveforms*

*Astable Operation*

(a) Resistors R1 and R2 give a potential divider bias for the transistor Q1. Re is the emitter resistor, whose job is to provide thermal stability for the transistor. Ce is the emitter by pass capacitors, which by-passes the amplified AC signals. If the emitter by-pass capacitor not there, the amplified ac voltages will drop across Re and it will get added on to the base-emitter voltage of Q1 and will disrupt the biasing conditions. Cin is the input DC decoupling capacitor while Cout is the output DC decoupling capacitor. The task of a DC decoupling capacitor is to prevent DC voltages from reaching the succeeding stage. Inductor L1, L2 and capacitor C1 forms the tank circuit.When the power supply is switched ON the transistor starts conducting and the collector current increases. As a result the capcitor C1 starts charging and when the capacitor C1 is fully charged it starts discharging through coil L1. This charging and discharging creates a series of damped oscillations in the tank circuit and it is the key.The oscillations produced in the tank circuit is coupled (fed back) to the base of Q1 and it appears in the amplified form across the collector and emitter of the transistor. The output voltage of the transistor (voltage across collector and emitter) will be in phase with the voltage across inductor L1. Since the junction of two inductors is grounded, the voltage across L2 will be 180° out of phase to that of the voltage across L1. The voltage across L2 is actually fed back to the base of Q1. From this we can see that, the feed back voltage is 180° out of phase with the transistor and also the transistor itself will create another 180° phase difference. So the total phase difference between input and output is 360° and it is very important condition for creating sustained oscillations.