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THIRD SEMESTER DIPLOMA EXAMINATION IN ELECTRICAL & ELECTRONICS ENGINEERING, MARCH 2013

ELECTRONIC DEVICES AND CIRCUITS

Time :3hours Maximum marks:100

PART A (maximum marks 10)

I. Answer the following questions in 2 or 3 sentences:

1A the charge carriers have the tendency to move from the region of higher concentration to that of lower concentration of the same type of charge carriers. Thus the movement of charge carriers takes place resulting in a current called diffusion current

2A voltage regulator,peak clipper,meter protection etc

3A The variation of dc output voltage output as a function of dc load current is called regulation. Percentage regulation is given as **% regulation = $V_{NL} - V_{FL} / V_{FL}$ *100**

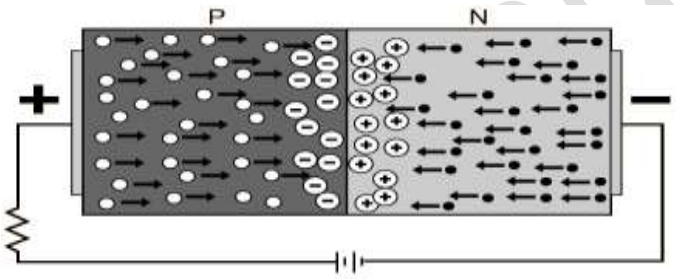
4A RC coupling,transformer coupling,inductor coupling,direct coupling

5A comparator,level detector

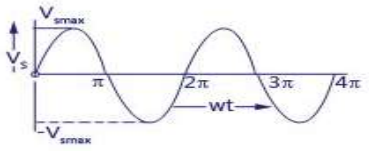
PART B (Maximum marks :30)

II Answer any five questions from the following

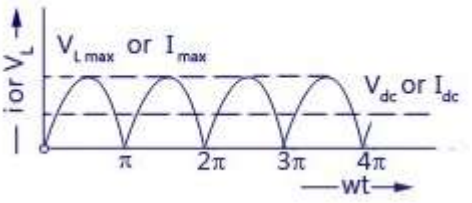
1A If an external voltage is connected in such a way that the P region terminal is connected to the positive of DC voltage and the N region is connected to the negative of the DC voltage, the biasing condition is called forward biasing. When we apply an external voltage more than the barrier potential, the negative terminal of battery pushes the electrons against barrier from N to P region. Similarly positive terminal pushes the holes from P to N region. Thus holes get repelled by positive terminal and cross the junction against barrier potential. This reduces the width of depletion region. As forward voltage increased, at a particular value the depletion region becomes very much narrow such that large number of charge carriers can cross the junction.In this way the flow of charge increases through the diode by increasing the applied voltage. The motion of charge particles can be observed in below picture.

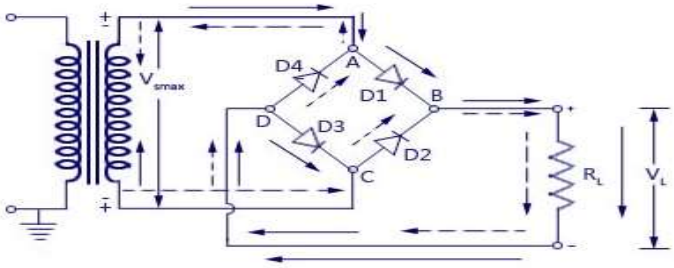


2A During first half cycle of the input voltage, the upper end of the transformer secondary winding is positive with respect to the lower end. Thus during the first half cycle diodes D1 and D_3 are forward biased and current flows through arm AB, enters the load resistance R_L, and returns back flowing through arm DC. During this half of each input cycle, the diodes D_2 and D_4 are reverse biased and current is not allowed to flow in arms AD and BC. The flow of current is indicated by solid arrows in the figure above. We have developed another diagram below to help you understand the current flow quickly. During second half cycle of the input voltage, the lower end of the transformer secondary winding is positive with respect to the upper end. Thus diodes D_2 and D_4 become forward biased and current flows through arm CB, enters the load resistance R_L, and returns back to the source flowing through arm DA. Flow of current has been shown by dotted arrows in the figure. Thus the direction of flow of current through the load resistance R_L remains the same during both half cycles of the input supply voltage

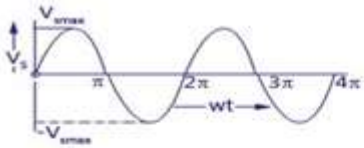


Input Voltage Waveform

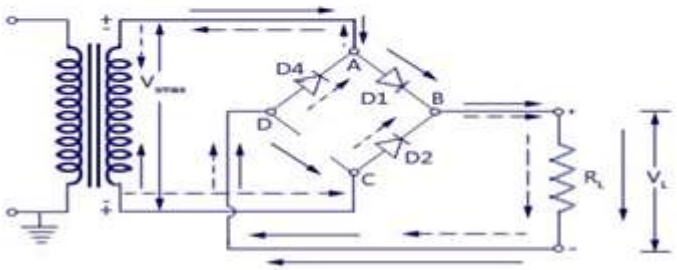


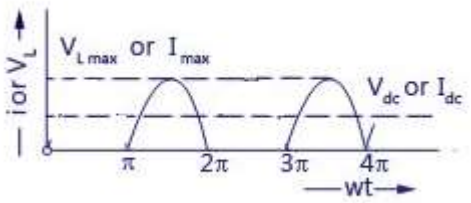


4A



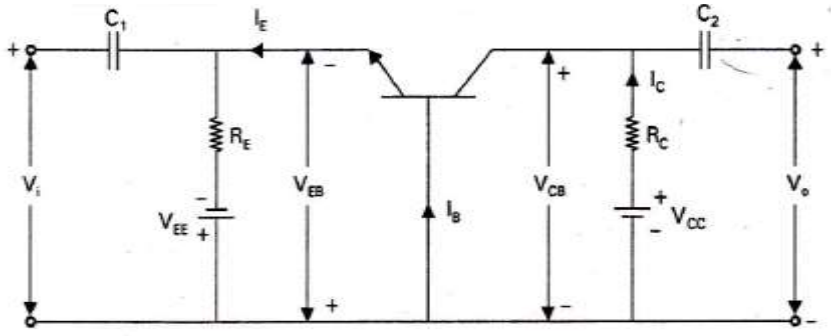
Input Voltage Waveform

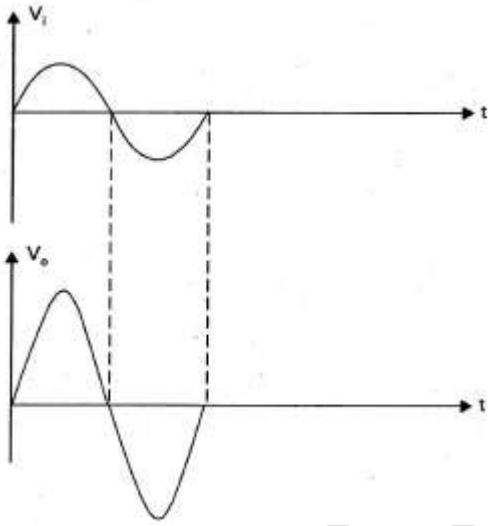




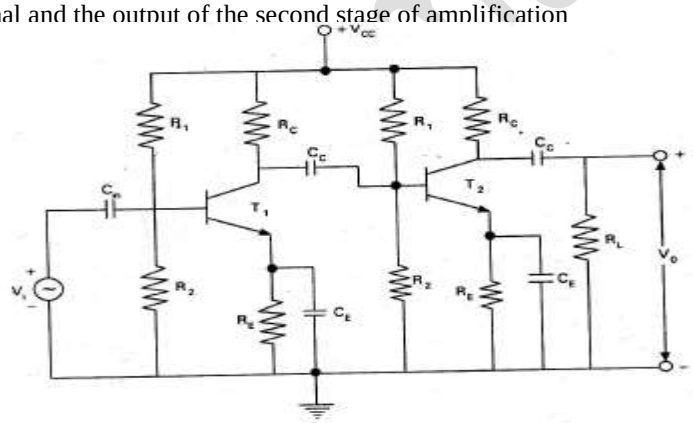
During +ve half cycle of the input signal comes then D1 is forward biased which conducts andcurrent flows from point A to point D via R_L,but from D to C it is open circuited .That makes the circuit incomplete. so the current at the starting time will not be able to complete the circuit so there will not be any output (0 to π, 2π to 3π…).During -ve half cycle D4 and D2 will conduct and which is shown in the figure.

4A The emitter base junction is forward biased by power supply VEE, and the collector-base junction is reverse biased by Vcc. So, the transistor remains in the active region throughout its operation. C1 and C2 are coupling capacitors to provide d.c. isolation at the input and output of the amplifier. When a sinusoidal a.c. signal is applied at the input, during the positive half cycle of the applied signal, the amount of forward bias to base-emitter junction is decreased, resulting in a decrease in Is and hence Ic also decreases. The drop lc Rc decreases, hence Vs Vco correspondingly increases. Thus, a positive-going input signal produces a positive-going output signal, there is no phase reversal between the two. During the negative half cycle of the input signal, the forward bias to emitter-base junction is increased, resulting in a increase in Ie and hence lc also increases. So, the drop lc Rc increases and hence Vo decreases.



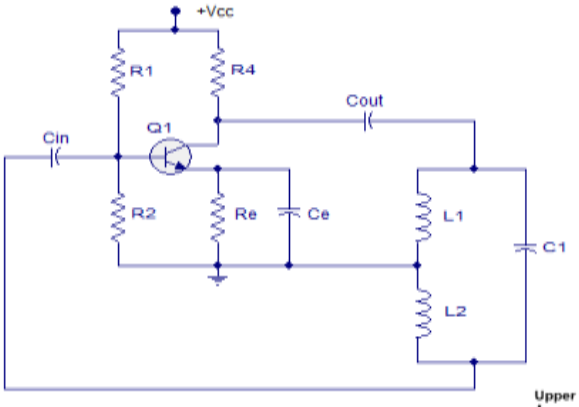


5A When an ac signal is applied to the input of first stage, it gets amplified by this stage and appears across the collector resistor itc of first-stage: This output voltage of first-stage is coupled to the base of the second stage through the coupling capacitor C. The amplified signal of first stage gets further amplification by the second stage and hence more amplification takes place. The output of the stage is taken out through the coupling the overall gain of amplification is equal so product of the individual stage gains. Av = Av1 * Av2 It Is to be noted that as the configuration employed Is CE configuration, each stage of amplification produces a phase shift of the input signal by 180. The overall phase shift is 2 x 180,or 360° or there's no phase difference between the input signal and the output of the second stage of amplification



6A Resistors R1 and R2 give a potential divider bias for the transistor Q1. Re is the emitter resistor, whose job is to provide thermal stability for the transistor. Ce is the emitter by pass capacitors, which by-passes the amplified AC signals. If the emitter by-pass capacitor not there, the amplified ac voltages will drop across Re and it will get added on to the base-emitter voltage of Q1 and will disrupt the biasing conditions. Cin is the input DC decoupling capacitor while Cout is the output DC decoupling capacitor. The task of a DC decoupling capacitor is to prevent DC voltages from reaching the succeeding stage. Inductor L1, L2 and capacitor C1 forms the tank circuit.When the power supply is switched ON the transistor starts conducting and the collector current increases. As a result the capcitor C1 starts charging and when the capacitor C1 is fully charged it starts discharging through coil L1. This charging and discharging creates a series of damped oscillations in the tank circuit and it is the key.The oscillations produced in the tank circuit is coupled (fed back) to the base of Q1 and it appears in the amplified form across the collector and emitter of the transistor. The output voltage of the transistor (voltage across collector and emitter) will be in phase

with the voltage across inductor L1. Since the junction of two inductors is grounded, the voltage across L2 will be 180° out of phase to that of the voltage across L1. The voltage across L2 is actually fed back to the base of Q1. From this we can see that, the feed back voltage is 180° out of phase with the transistor and also the transistor itself will create another 180° phase difference. So the total phase difference between input and output is 360° and it is very important condition for creating sustained oscillations.



7A

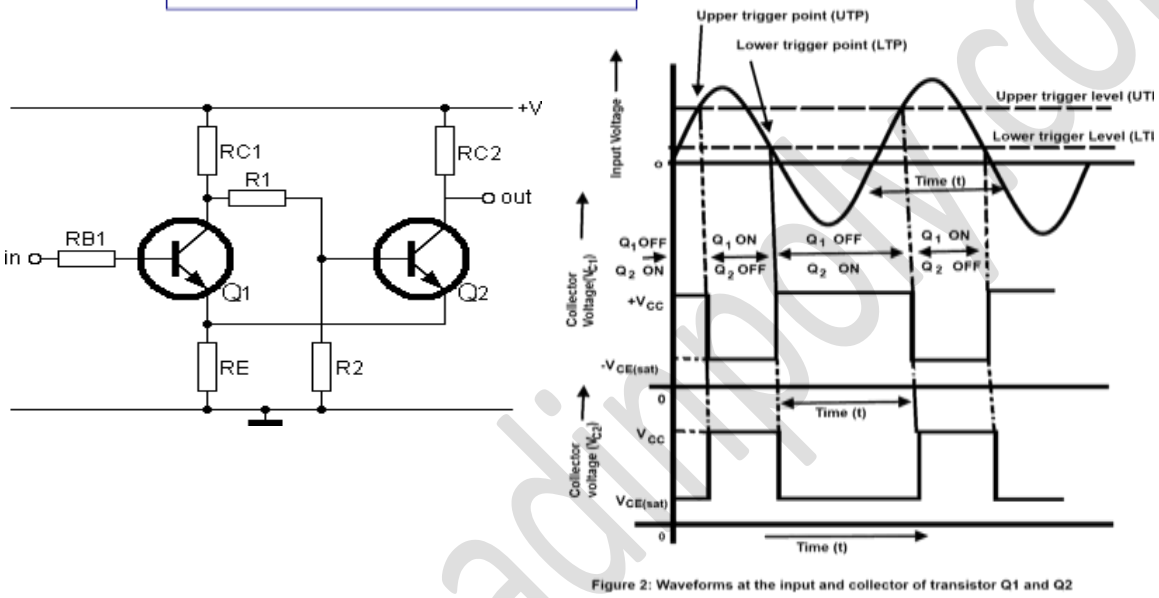


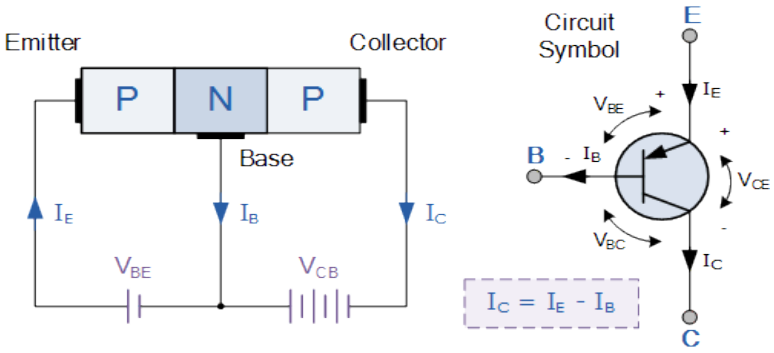
Figure 2: Waveforms at the input and collector of transistor Q1 and Q2

A.C. signal is applied at the input of the Schmitt trigger (i.e. at the base of the transistor Q_1). As the input voltage increases above zero, nothing will happen till it crosses the upper trigger level (U.L.T). As the input voltage increases, above the upper trigger level, the transistor Q_1 conducts. The point, at which it starts conducting, is known as upper trigger point (U.T.P). As the transistor Q_1 conducts, its collector voltage falls below V_{CC}. This fall is coupled through resistor R_1 to the base of transistor Q_2 which reduces its forward bias. This in turn reduces the current of transistor Q_2 and hence the voltage drop across the resistor R_E. As a result of this, the reverse bias of transistor Q_1 is reduced and it conducts more. As the transistor Q_1 conducts more heavily, its collector further reduces due to which the transistor Q_1 conducts near cut-off. This process continues till the transistor Q_1 is driven into saturation and Q_2 into cut-off. At this instant, the collector voltage levels are $V_{C1} = V_{CE(sat)}$ and $V_{C2} = V_{CC}$ as shown in the figure.The transistor Q_1 will continue to conduct till the input voltage falls below the lower trigger level (L.T.L). It will be interesting to know that when the input voltage becomes equal to the lower trigger level, the emitter base junction of transistor Q_1 becomes reverse biased. As a result of this, its collector voltage starts rising toward V_{CC}. This rising voltage increases the forward bias across transistor Q_2 due to which it conducts. The point, at which transistor Q_2 starts conducting, is called lower trigger point (L.T.P). Soon the transistor Q_2 is driven into saturation and Q_1 to cur-off. This completes one cycle. The collector voltage levels at this instant are $V_{C1} = V_{CC}$ and $V_{C2} = V_{CE(sat)}$. No change in state will occur during the negative half cycle of the input voltage.

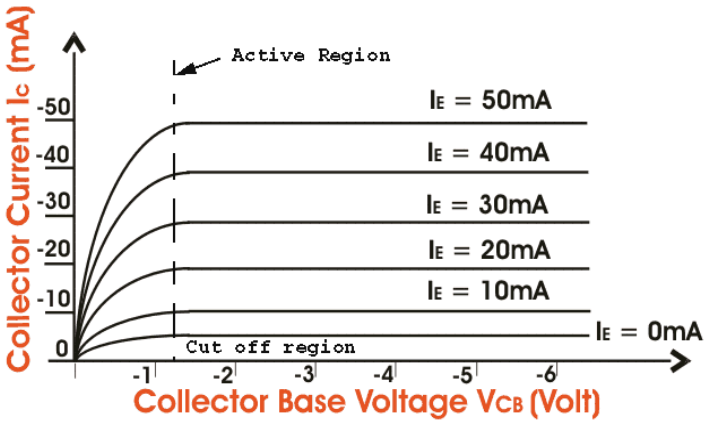
PART C

III (a) The positive voltage on the emitter repels the holes toward the base. Once in the base, the holes combine with base electrons. But again, remember that the base region is made very thin to prevent the recombination of holes with electrons. Therefore, well over 90 percent of the holes that enter the base become attracted to the large negative collector voltage and pass right through the base. However, for each electron and hole that combine in the base region, another electron leaves the negative terminal of the base battery (V_{BB}) and enters the base as base current (I_B). At the same time an electron leaves the negative terminal of the battery, another electron leaves the emitter as IE (creating a new hole) and enters the positive terminal of V_{BB}. Meanwhile, in the collector circuit, electrons from the collector battery (V_{CC}) enter the collector as Ic and combine with the excess holes from the base. For each hole that is neutralized in the collector by an electron, another electron leaves the emitter and starts its way back to the positive terminal of V_{CC}.Although current flow in the external circuit of the *pnp* transistor is opposite in

direction to that of the *npn* transistor, the majority carriers always flow from the emitter to the collector. This flow of majority carriers also results in the formation of two individual current loops within each transistor. One loop is the base-current path, and the other loop is the collector-current path. The combination of the current in both of these loops ($I_B + I_C$) results in total transistor current (I_E). In simple terms, increasing the forward-bias voltage of a transistor reduces the emitter-base junction barrier. This action allows more carriers to reach the collector, causing an increase in current flow from the emitter to the collector and through the external circuit. Conversely, a decrease in the forward-bias voltage reduces collector current.



(b) The output characteristics shows the relation between output voltage and output current I_C is the output current and collector – base voltage and the emitter current I_E is the input current and works as the parameters. The figure below shows the output characteristics for a p - n - p transistor in CB mode. As we know for p - n - p transistors I_E and V_{EB} are positive and I_C, I_B, V_{CB} are negative. These are three regions in the curve, active region saturation region and the cut off region. The active region is the region where the transistor operates normally. Here the emitter junction is reverse biased. Now the saturation region is the region where both the emitter collector junctions are forward biased. And finally the cut off region is the region where both emitter and the collector junctions are reverse biased.



IV (a)

We know that, $I_E = I_C + I_B$ ... (1)

divide the above equation by I_C, we get

$$\frac{I_E}{I_C} = \frac{I_C}{I_C} + \frac{I_B}{I_C}$$

$$\frac{1}{\alpha} = 1 + \frac{1}{\beta}$$

$$\frac{1}{\beta} = \frac{1}{\alpha} - 1 = \frac{1-\alpha}{\alpha}$$

$$\therefore \quad \boxed{\beta = \frac{\alpha}{1-\alpha}} \qquad \text{... (2)}$$

from eq. (1), $I_B = I_E - I_C$

$$\therefore \quad \gamma = \frac{I_E}{I_B} = \frac{I_E}{I_E - I_C}$$

dividing the N.R and D.R on RHS by I_E, we get

$$\gamma = \frac{I_E/I_E}{\frac{I_E}{I_E} - \frac{I_C}{I_E}} = \frac{1}{1-\alpha}$$

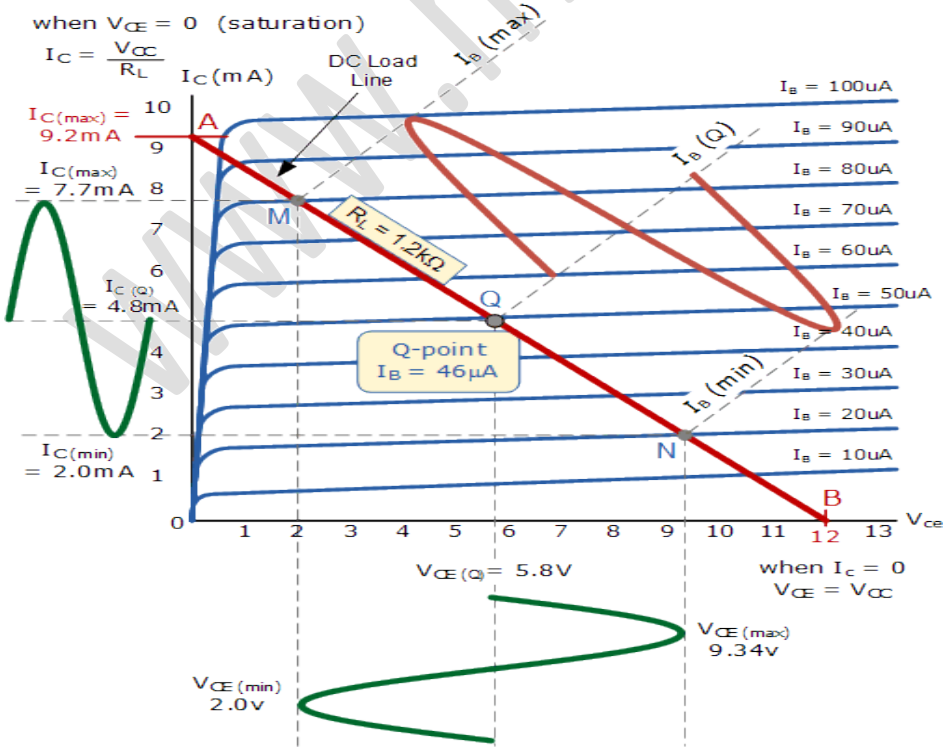
$$\therefore \quad \boxed{\gamma = \frac{1}{1-\alpha}}$$

Adding 1 to eq. (2) on both sides, we get

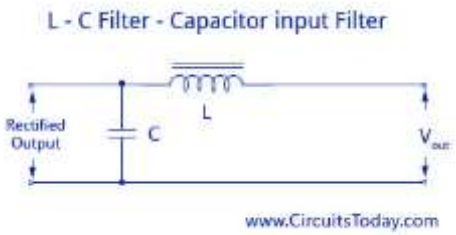
$$\beta + 1 = \frac{\alpha}{1-\alpha} + 1 = \frac{\alpha + 1 - \alpha}{1-\alpha} = \frac{1}{1-\alpha} = \gamma$$

$$\therefore \quad \gamma = \beta + 1.$$

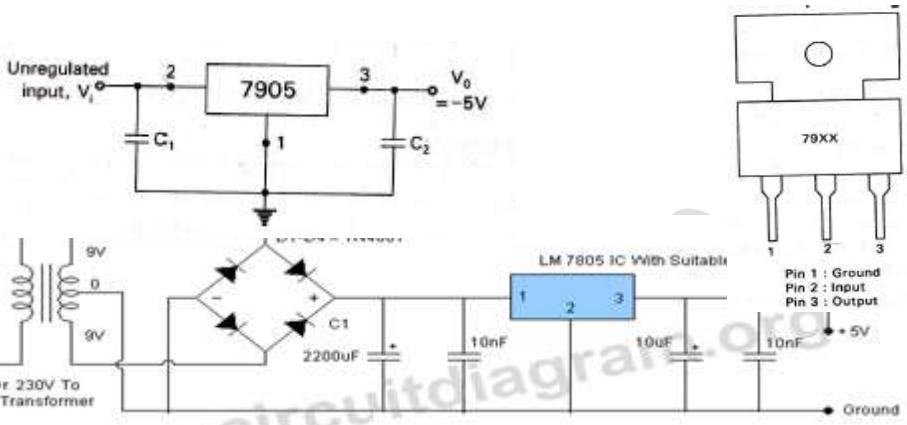
(b) As the load line cuts through the different Base current values on the DC characteristics curves we can find the peak swings of Base current that are equally spaced along the load line. These values are marked as points N and M on the line, giving a minimum and a maximum Base current of 20µA and 80µA respectively.These points, N and M can be anywhere along the load line that we choose as long as they are equally spaced from Q. This then gives us a theoretical maximum input signal to the Base terminal of 60µA peak-to-peak, (30µA peak) without producing any distortion to the output signal.Any input signal giving a Base current greater than this value will drive the transistor to go beyond point N and into its "cut-off" region or beyond point M and into its Saturation region thereby resulting in distortion to the output signal in the form of "clipping".Using points N and M as an example, the instantaneous values of Collector current and corresponding values of Collector-emitter voltage can be projected from the load line. It can be seen that the Collector-emitter voltage is in anti-phase (-180°) with the collector current.As the Base current Ib changes in a positive direction from 50µA to 80µA, the Collector-emitter voltage, which is also the output voltage decreases from its steady state value of 5.8v to 2.0v.Then a single stage **Common Emitter Amplifier** is also an "Inverting Amplifier" as an increase in Base voltage causes a decrease in Vout and a decrease in Base voltage produces an increase in Vout. In other words the output signal is 180° out-of-phase with the input signal.



V (a) The name pi – Filter implies to the resemblance of the circuit to a Π shape with two shunt capacitances (C1 and C2) and an inductance filter 'L'. As the rectifier output is provided directly into the capacitor it also called a capacitor input filter.The output from the rectifier is first given to the shunt capacitor C. The rectifier used can be half or full wave and the capacitors are usually electrolytic even though they large in size. In practical applications, the two capacitances are enclosed in a metal container which acts as a common ground for the two capacitors. The Π – Filter has some advantages like higher dc voltage and smaller ripple factor. But it also has some disadvantages like poor voltage regulation, high peak diode current, and high peak inverse voltage.This filter is divided into two – a capacitor filter and a L-section filter. The capacitor C1 does most of the filtering in the circuit and the remaining ripple os removed by the L-section filter (L-C2). C1 is selected to provide very low reactance to the ripple frequency. The voltage regulation is poor for this circuit as the output voltage falls off rapidly with the increase in load current.

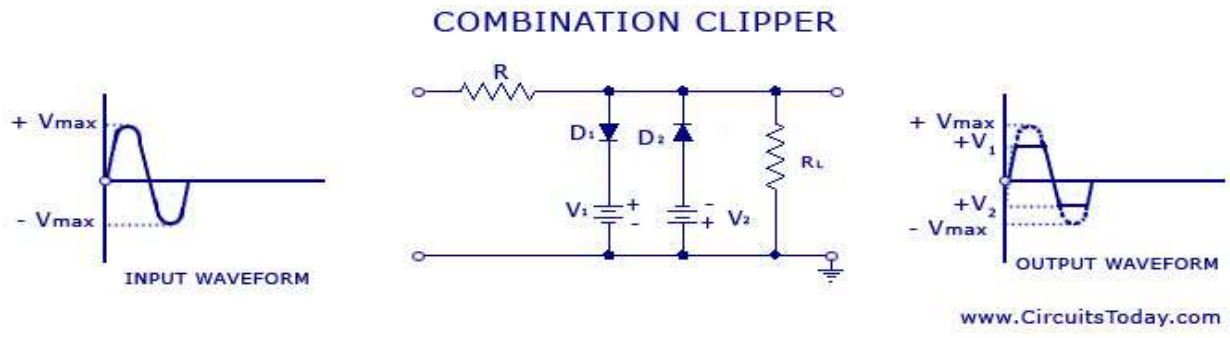


(b)



pin 2 is the input terminal, pin 1 is the ground and pin 3 is the output terminal. The unregulated input voltage (V1) is given to the input terminal. The output is taken from the output terminal. Filter capacitors are shown to be connected at the input and output side. The input capacitor C1 is used to cancel the inductive effects due to long distiibution leads and the output capacitor C2 improves the transient response.

VI (a) When a portion of both positive and negative of each half cycle of the input voltage is to be clipped (or removed), combination clipper is employed. The circuit for such a clipper is given in the figure below.



The action of the circuit is summarized below. For positive input voltage signal when input voltage exceeds battery voltage '+ V_1' diode D_1 conducts heavily while diode 'D_2' is reversed biased and so voltage '+ V_1' appears across the output. This output voltage '+ V_1' stays as long as. the input signal voltage exceeds '+ V_1'. On the other hand for the negative input voltage signal, the diode 'D_1' remains reverse biased and diode 'D_2' conducts heavily only when input voltage exceeds battery voltage 'V_2' in magnitude. Thus during the negative half cycle the output stays at '- V_2' so long as the input signal voltage is greater than '-V_2'.

(b) It consists of a diode and a capacitor the clamper output is taken across the load resistance R.

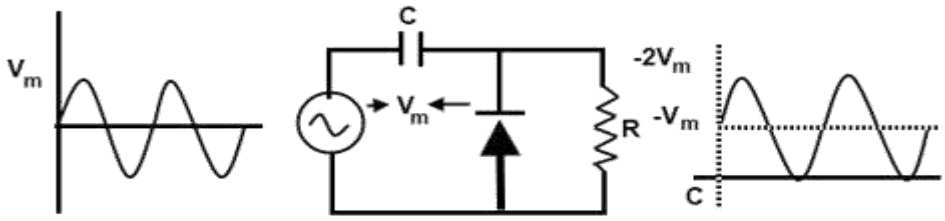
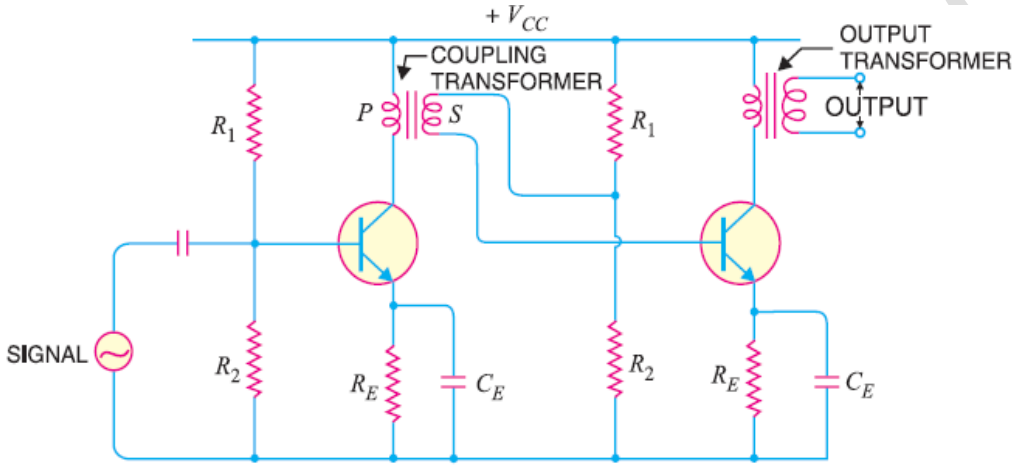
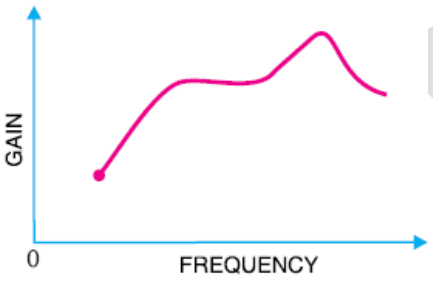


Fig. 2 Positive Clamper

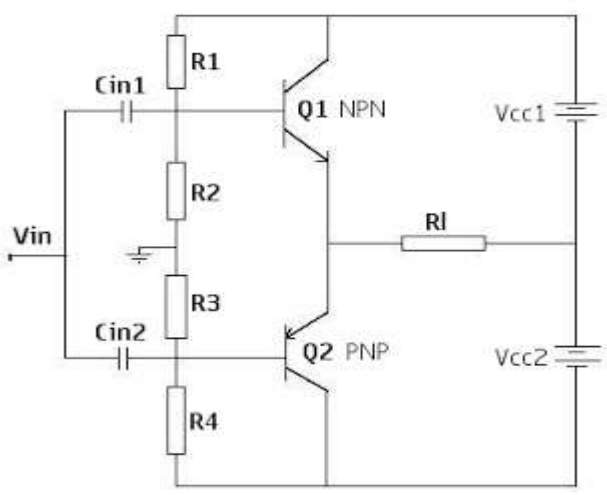
During the negative half cycle of the input voltage, the diode conducts heavily and behaves as a closed switch At the negative peak, the capacitor is charged to maximum voltage V slightly beyond the negative peak, the diode is shunt off and the capacitor charged to Vm behaves as a battery during the positive half cycle of the input signal. The diode is reversed biased and the output voltage will be equal to Vm + V this gives positive clamped voltage and is called positive clamper circuit.

VII (a)





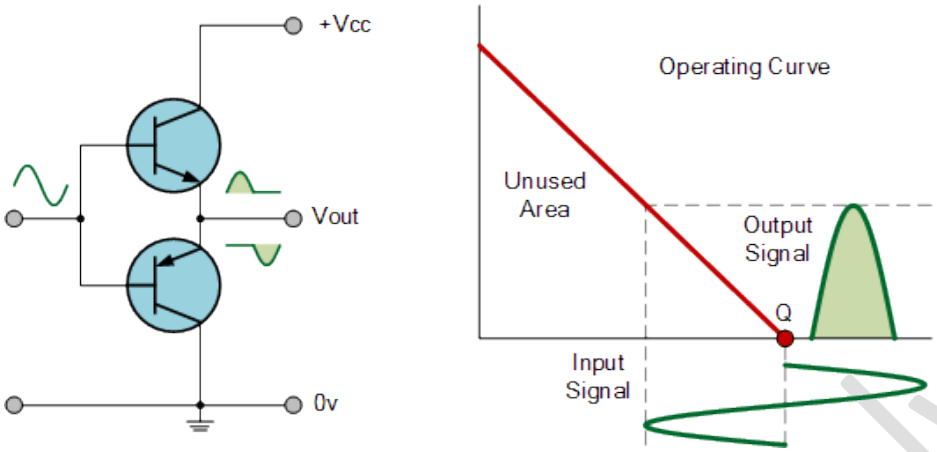
It is clear that frequency response is rather poor i.e. gain is constant only over a small range of frequency. The out-put voltage is equal to the collector current multiplied by reactance of primary. At low frequencies, the reactance of primary begins to fall, resulting in decreased gain. At high frequencies, the capacitance between turns of windings acts as a bypass condenser to reduce the output voltage and hence gain. It follows, therefore, that there will be disproportionate amplification of frequencies in a complete signal such as music, speech etc. Hence, transformer-coupled amplifier introduces frequency distortion. It may be added here that in a properly designed transformer, it is possible to achieve a fairly constant gain over the audio frequency range. But a transformer that achieves a frequency response comparable to RC coupling may cost 10 to 20 times as much as the inexpensive RC coupled amplifier.



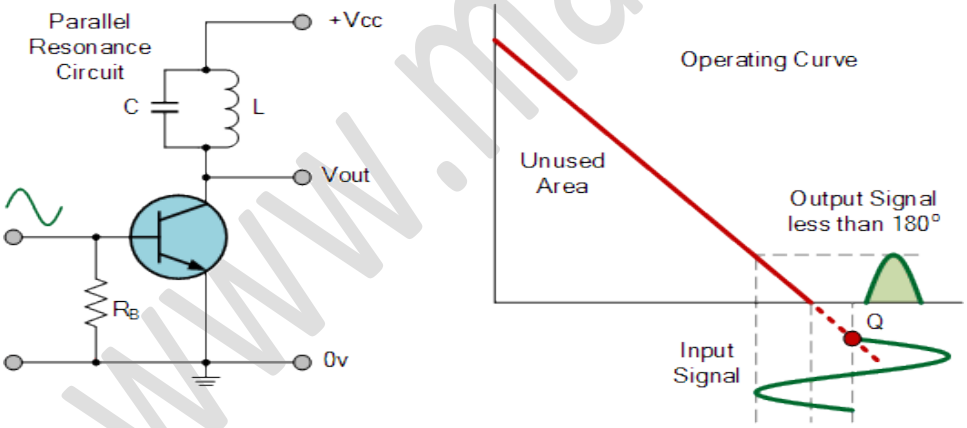
(b)

The signal applied at the input goes to the base of both the transistors. The two transistors conduct in the opposite half cycle of input signal, the NPN transistor Q1 is forward biased and conducts while the PNP transistor Q2 is reverse biased and so does not conduct. This results in a half cycle of output voltage across the load, resistor Rl. Similarly during the negative half cycle only the PNP transistor Q2 is forward biased and conducts which develops second half cycle of the output voltage across the Load Resistor Rl. Transistor Q1 being reverse biased and does not conduct during the negative half cycle of the input signal. Thus during a complete cycle of input, a complete cycle of output will developed.

VIII (a)

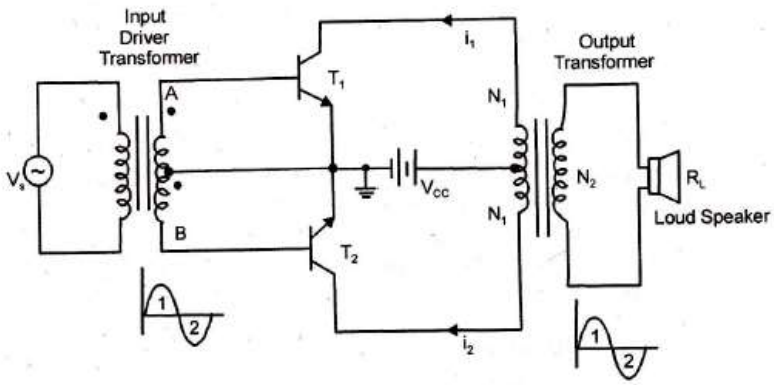


When the input signal goes positive, the positive biased transistor conducts while the negative transistor is switched “OFF”. Likewise, when the input signal goes negative, the positive transistor switches “OFF” while the negative biased transistor turns “ON” and conducts the negative portion of the signal. Thus the transistor conducts only half of the time, either on positive or negative half cycle of the input signal. The class B amplifier only conducts through one half or 180 degrees of the output waveform in strict time alternation, but as the output stage has devices for both halves of the signal waveform the two halves are combined together to produce the full linear output waveform. This push-pull design of amplifier is obviously more efficient than Class A, at about 50%, but the problem with the class B amplifier design is that it can create distortion at the zero-crossing point of the waveform due to the transistors dead band of input base voltages from -0.7V to +0.7.It takes a base-emitter voltage of about 0.7 volts to get a bipolar transistor to start conducting. Then in a class B amplifier, the output transistor is not “biased” to an “ON” state of operation until this voltage is exceeded. To overcome this zero-crossing distortion (also known as Crossover Distortion) class AB amplifiers were developed.



Due to its heavy audio distortion, class C amplifiers are commonly used in high frequency sine wave oscillators and certain types of radio frequency amplifiers, where the pulses of current produced at the amplifiers output can be converted to complete sine waves of a particular frequency by the use of LC resonant circuits in its collector circuit.

(b)

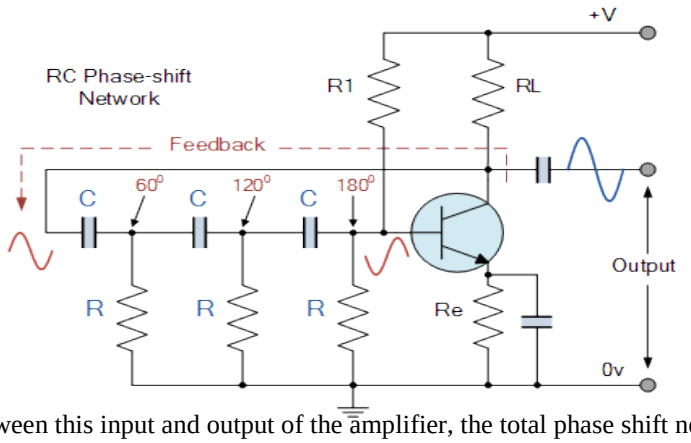


The input signal appears across the secondary AB of driver transformer. During the positive half cycle of the signal, end A becomes positive and end B negative. This will make the base - emitter junction of T, forward biased and that of T, reverse biased. The circuit will conduct current due to T, only, and is shown by current i,. Therefore, this half-cycle of the signal is amplified by T, and appears in the upper half of the primary of output transformer. During the negative half - cycle of the input signal, T2 is forward biased whereas T, is reverse biased. Therefore, T2 conducts and is shown by current i2. So, this half - cycle of the signal is amplified by T2 and appears in the lower half of the output transformer primary. The centre tapped primary of the output transformer combines two collector currents to form a sine wave output in the secondary. Thus the two transistors conduct in alternate half cycles of the input signal. Hence the collector current flow in opposite direction. So the net d.c in the primary is zero. However, the secondary of the output transformer will have induced voltage. Output of the amplifier will be twice that of the output offered by the single transistor. The push - pull arrangement also permits a maximum transfer of power to the load through impedance matching. The turns ratio 2 N, : N2 of the transformer is chosen so that the load R_L is matched with the output impedance of the transistor. If R_L is the resistance connected across the secondary of output transformer, then the resistance looking into the primary is

$$R_L^1 = \left(\frac{2N_1}{N_2}\right)^2 R_L$$

IX (a) The basic **RC Oscillator** which is also known as a **Phase-shift Oscillator**, produces a sine wave output signal using regenerative feedback obtained from the resistor-capacitor combination. This regenerative feedback from the RC network is due to the ability of the capacitor to store an electric charge, (similar to the LC tank circuit).This resistor-capacitor feedback network can be connected as shown above to produce a leading phase shift (phase advance network) or interchanged to produce a lagging phase shift (phase retard network) the outcome is still the same as the sine wave oscillations only occur at the frequency at which the overall phase-shift is 360^o.By varying one or more of the resistors or capacitors in the phase-shift network, the frequency can be varied and generally this is done by keeping the resistors the same and using a 3-ganged variable capacitor.If all the resistors, R and the capacitors, C in the phase shift network are equal in value, then the frequency of oscillations produced by the RC oscillator is given as:

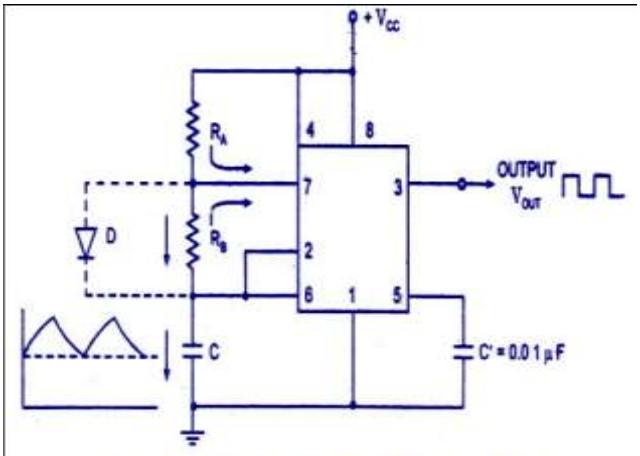
$$f_r = \frac{1}{2\pi RC\sqrt{2N}}$$



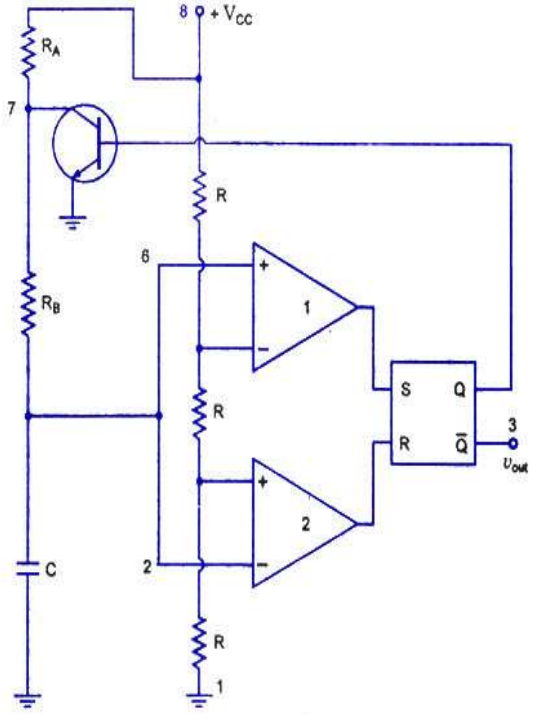
If a three-stage RC phase-shift network is connected between this input and output of the amplifier, the total phase shift necessary for regenerative feedback will become 3 x 60^o + 180^o = 360^o

(b) when Q is low or output V_{OUT} is high, the discharging transistor is cut-off and the capacitor C begins charging toward V_{CC} through resistances R_A and R_B. Because of this, the charging time constant is (R_A + R_B) C. Eventually, the threshold voltage exceeds +2/3 V_{CC}, the comparator 1 has a high output and triggers the flip-flop so that its Q is high and the timer output is low. With Q high, the discharge transistor saturates and pin 7 grounds so that the capacitor C discharges through resistance R_B with a discharging time constant R_B C. With the discharging of capacitor, trigger voltage at inverting input of comparator 2 decreases.

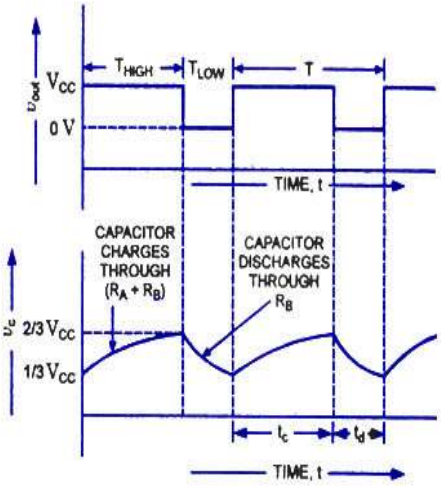
When it drops below $1/3V_{CC}$, the output of comparator 2 goes high and this reset the flip-flop so that Q is low and the timer output is high. This proves the auto-transition in output from low to high and then to low as, illustrated in fig ures. Thus the cycle repeats.



Circuit of The Timer 555 as an Astable Multivibrator



Internal Circuitry With External Connections

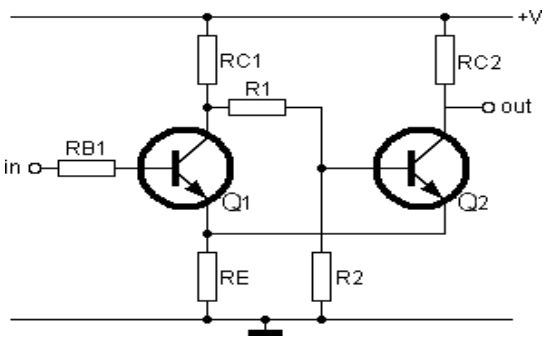


Capacitor and Output Voltage Waveforms

Astable Operation

X

(a)



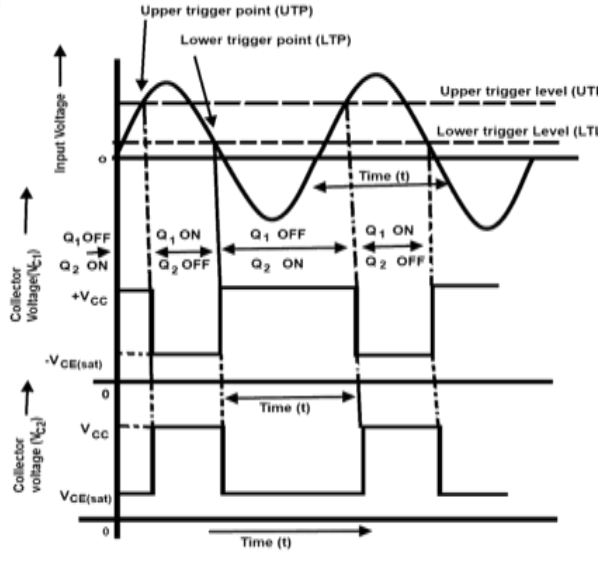
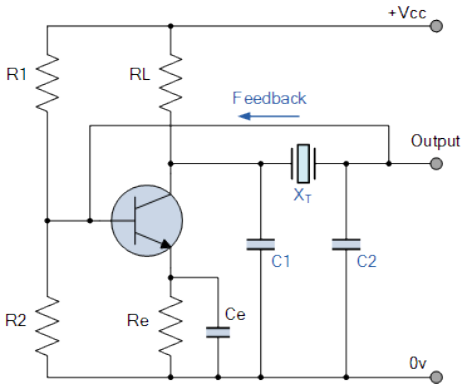
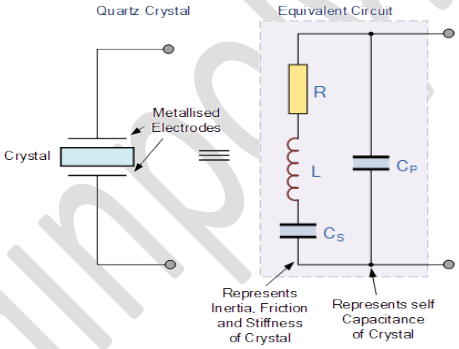


Figure 2: Waveforms at the input and collector of transistor Q1 and Q2

A.C. signal is applied at the input of the Schmitt trigger (i.e. at the base of the transistor Q_1). As the input voltage increases above zero, nothing will happen till it crosses the upper trigger level (U.L.T). As the input voltage increases, above the upper trigger level, the transistor Q_1 conducts. The point, at which it starts conducting, is known as upper trigger point (U.T.P). As the transistor Q_1 conducts, its collector voltage falls below V_{CC}. This fall is coupled through resistor R_1 to the base of transistor Q_2 which reduces its forward bias. This in turn reduces the current of transistor Q_2 and hence the voltage drop across the resistor R_E. As a result of this, the reverse bias of transistor Q_1 is reduced and it conducts more. As the transistor Q_1 conducts more heavily, its collector further reduces due to which the transistor Q_1 conducts near cut-off. This process continues till the transistor Q_1 is driven into saturation and Q_2 into cut-off. At this instant, the collector voltage levels are $V_{C1} = V_{CE(sat)}$ and $V_{C2} = V_{CC}$ as shown in the figure.The transistor Q_1 will continue to conduct till the input voltage falls below the lower trigger level (L.T.L). It will be interesting to know that when the input voltage becomes equal to the lower trigger level, the emitter base junction of transistor Q_1 becomes reverse biased. As a result of this, its collector voltage starts rising toward V_{CC}. This rising voltage increases the forward bias across transistor Q_2 due to which it conducts. The point, at which transistor Q_2 starts conducting, is called lower trigger point (L.T.P). Soon the transistor Q_2 is driven into saturation and Q_1 to cur-off. This completes one cycle. The collector voltage levels at this instant are $V_{C1} = V_{CC}$ and $V_{C2} = V_{CE(sat)}$. No change in state will occur during the negative half cycle of the input voltage.

(b) These types of **Crystal Oscillators** are designed around the common emitter amplifier stage of a **Colpitts Oscillator**. The input signal to the base of the transistor is inverted at the transistors output. The output signal at the collector is then taken through a 180^o phase shifting network which includes the crystal operating in a series resonant mode.The output is also fed back to the input which is "in-phase" with the input providing the necessary positive feedback. Resistors, R1 and R2 bias the resistor in a Class A type operation while resistor Re is chosen so that the loop gain is slightly greater than unity.





Capacitors, C1 and C2 are made as large as possible in order that the frequency of oscillations can approximate to the series resonant mode of the crystal and is not dependant upon the values of these capacitors.The circuit diagram above of the **Colpitts Crystal Oscillator** circuit shows that capacitors, C1 and C2 shunt the output of the transistor which reduces the feedback signal. Therefore, the gain of the transistor limits the maximum values of C1 and C2. The output amplitude should be kept low in order to avoid excessive power dissipation in the crystal otherwise could destroy itself by excessive vibration.