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THIRD SEMESTER DIPLOMA EXAMINATION IN ELECTRICAL & ELECTRONICS ENGINEERING, OCTOBER 2011
ELECTRONIC DEVICES AND CIRCUITS

Time :3hours Maximum marks:100

PART A (maximum marks 10)

I. Answer the following questions in 2 or 3 sentences: marks

1A drift current is defined as the flow of electric current due to the motion of the charge carriers under the influence of an external electric field.

2A when the applied voltage is so large that electrons that are pulled from their covalent bonds are accelerated to great velocities. These electrons collide with the silicon atoms and knock off more electrons. These electrons are then also accelerated and subsequently collide with other atoms. Each collision produces more electrons which leads to more collisions etc. The current in the semiconductor rapidly increases and the material can quickly be destroyed.

3A The conversion efficiency of a rectifier ckt is generally defined as
Na= dc power delivered to the load/ ac power input to the rectifier ckt. Or efficiency = Pdc/Pac

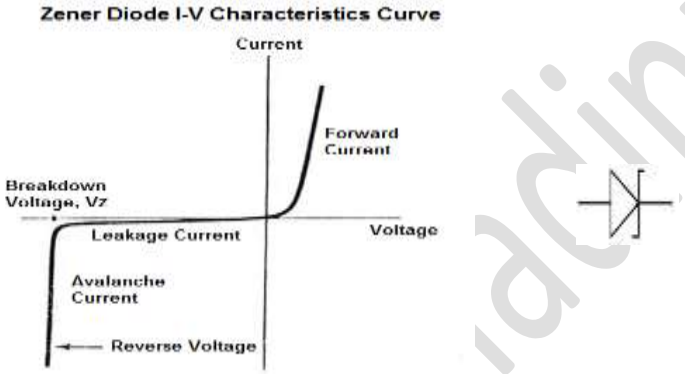
4A. class A, class B, class C, class AB

5A function generators,RF generators,digital clocks,computers.

PART B (Maximum marks :30)

II Answer any five questions from the following

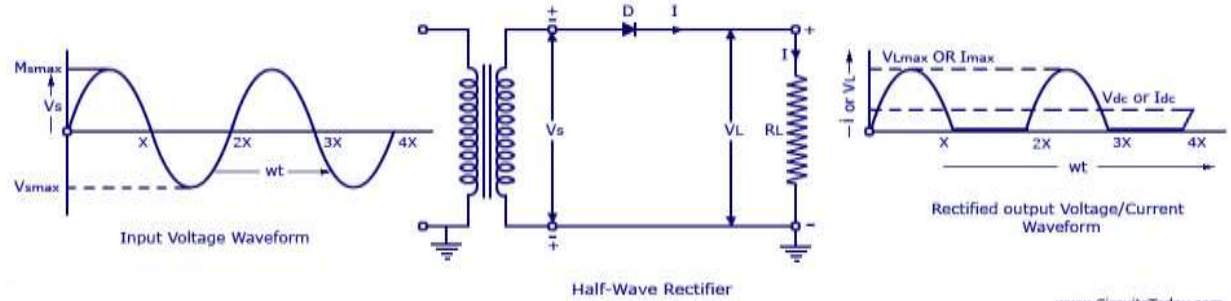
1 A



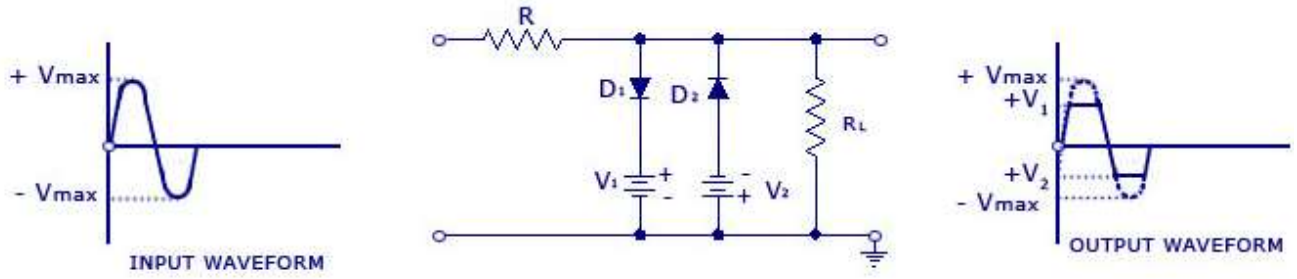
Forward characteristics of zener diode: is similar to that of an ordinary diode.

Reverse characteristics of zener diode: Under reverse biasing condition , only a very small current will flows its due to minority charge carriers.If the reverse bias voltage is made too high, the current through the pn junction increases rapidly. This is called break down voltage. At this voltage the crystal structure will breaks down. There are 2 break downs.When reverse bias is increased the electric field at the junction also increase. High electric field causes covalent bond to break.so no.of carriers are generated. This causes large current to flow. This is called zener break down.The increased electric field causes increase in the velocities of minority carriers.These high energy carriers break covalent bonds,there by generating more carriers.again these generated carriers are accelerated by the electric field.A chain reaction is thus established.This is called avalanche break down**.**

2A The input we give here is an alternating current. This input voltage is stepped down using a transformer. The reduced voltage is fed to the diode 'D' and load resistance RL. During the positive half cycles of the input wave, the diode 'D' will be forward biased and during the negative half cycles of input wave, the diode 'D' will be reverse biased. We take the output across load resistor RL. Since the diode passes current only during one half cycle of the input wave, we get an output as shown in diagram. The output is positive and significant during the positive half cycles of input wave. At the same time output is zero or insignificant during negative half cycles of input wave. This is called **half wave rectification**

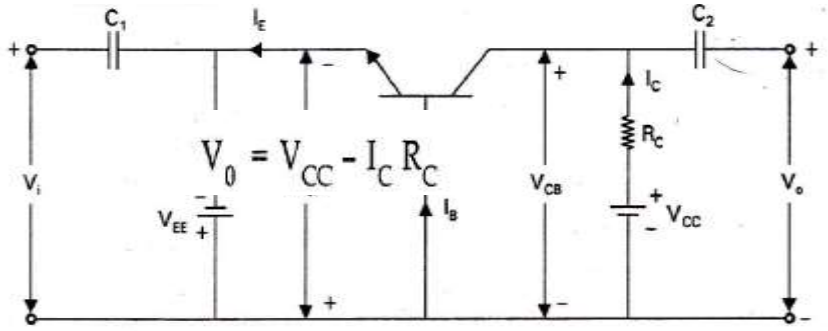


3 A

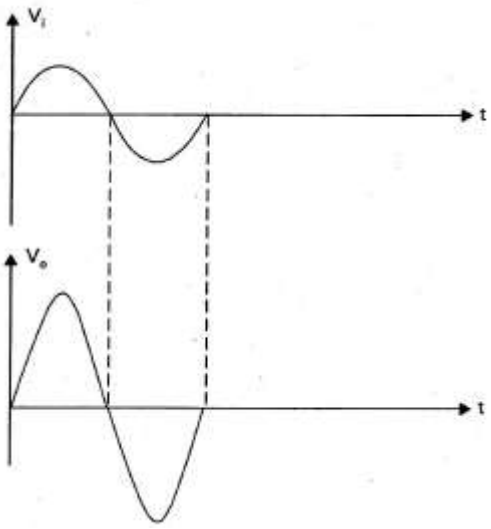


For positive input voltage signal when input voltage exceeds battery voltage '+ V_1' diode D_1 conducts heavily while diode 'D_2' is reversed biased and so voltage '+ V_1' appears across the output. This output voltage '+ V_1' stays as long as. the input signal voltage exceeds '+ V_1'. On the other hand for the negative input voltage signal, the diode 'D_1' remains reverse biased and diode 'D_2' conducts heavily only when input voltage exceeds battery voltage 'V_2' in magnitude. Thus during the negative half cycle the output stays at '- V_2' so long as the input signal voltage is greater than '-V_2'.

4A The emitter base junction is forward biased by power supply VEE, and the collector-base junction is reverse biased by Vcc. So, the transistor remains in the active region throughout its operation. C1 and C2 are coupling capacitors to provide d.c. isolation at the input and output of the amplifier.



When a sinusoidal a.c. signal is applied at the input, during the positive half cycle of the applied signal, the amount of forward bias to base-emitter junction is decreased, resulting in a decrease in Is and hence Ic also decreases. The drop lc Rc decreases, hence Vs Vco correspondingly increases. Thus, a positive-going input signal produces a positive-going output signal, there is no phase reversal between the two. During the negative half cycle of the input signal, the forward bias to emitter-base junction is increased, resulting in a increase in Ie and hence lc also increases. So, the drop lc Rc increases and hence Vo decreases.

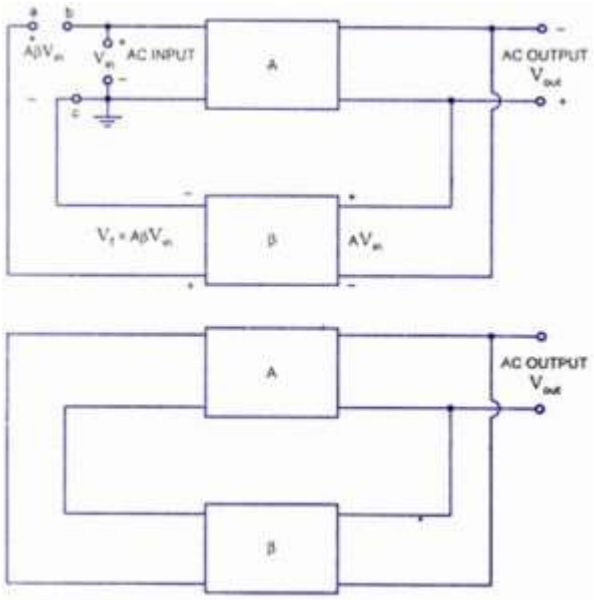


5A A feedback amplifier having closed-loop gain, A_f greater than unity can be obtained by the use of a positive feedback. This result also satisfies the phase condition and thus results in the operation of an oscillator circuit. An oscillator circuit then provides a constantly varying output signal. If the output signal varies sinusoidally, the circuit can be called as a sinusoidal oscillator. The amplified output voltage is $\mathbf{V_{out} = A V_{in}}$This voltage drives a feedback circuit that is usually a resonant circuit, as we get maximum feedback at one frequency. The feedback voltage returning to point a is given by equation $\mathbf{V_f = A \beta V_{in}}$ **where β is the gain of feedback network**.If the phase shift through the amplifier and feedback circuit is zero, then A β V_{in} is in phase with the input

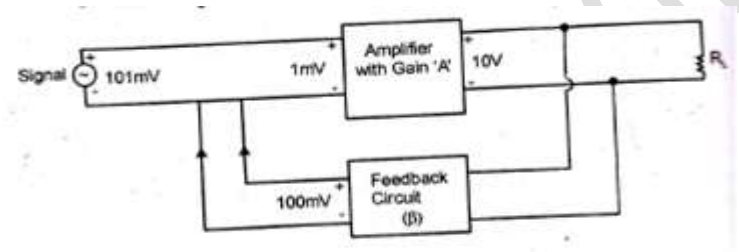
signal V_{in} that drives the input terminals of the amplifier.Certain conditions are required to be fulfilled for sustained oscillations and these conditions are that

(i) The loop gain of the circuit must be equal to (or greater than) unity and

(ii) The phase shift around the circuit must be zero. These two conditions for sustained oscillations are called Barkhausen *criteria*.

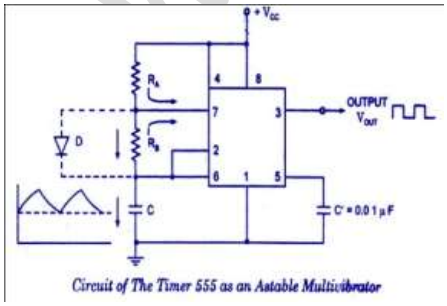


when any increase in the output signal results in a feedback signal into the input in such a way as to decrease the output signal the amplifier is said to have negative feedback.The output of the amplifier is 10v.The fraction beta of this output ie 100mV is feedback to the input where it is applied in series with the input signal of 101mV.As the feedback is negative only 1mV appears At the input terminals of the amplifier.

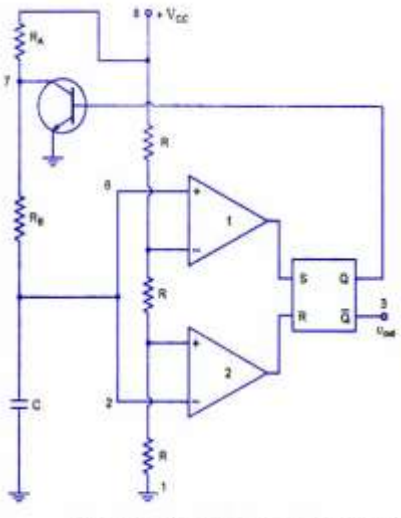


$$G = \frac{A}{1 + \beta A}$$

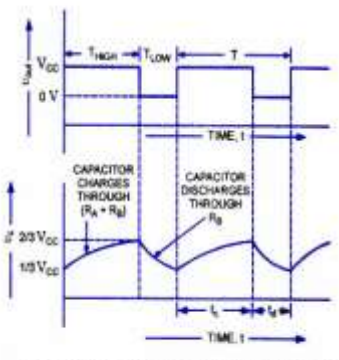
6A. when Q is low or output V_{OUT} is high, the discharging transistor is cut-off and the capacitor C begins charging toward V_{CC} through resistances R_A and R_B. Because of this, the charging time constant is $(R_A + R_B)$ C. Eventually, the threshold voltage exceeds +2/3 V_{CC}, the comparator 1 has a high output and triggers the flip-flop so that its Q is high and the timer output is low. With Q high, the discharge transistor saturates and pin 7 grounds so that the capacitor C discharges through resistance R_B with a discharging time constant R_B C. With the discharging of capacitor, trigger voltage at inverting input of comparator 2 decreases. When it drops below 1/3V_{CC}, the output of comparator 2 goes high and this reset the flip-flop so that Q is low and the timer output is high. This proves the auto-transition in output from low to high and then to low as, illustrated in fig ures. Thus the cycle repeats.



Circuit of The Timer 555 as an Astable Multivibrator

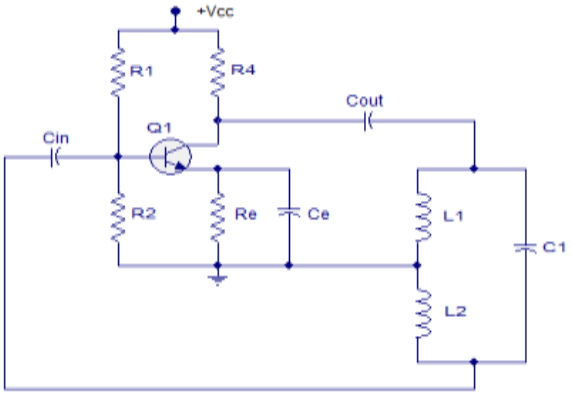


Internal Circuitry With External Connections



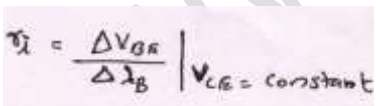
Capacitor and Output Voltage Waveforms

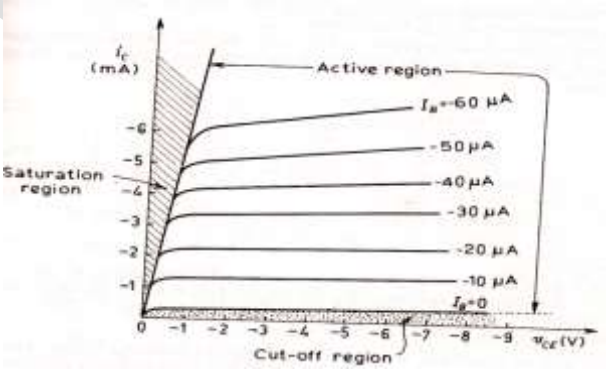
7A. resistors R1 and R2 give a potential divider bias for the transistor Q1. Re is the emitter resistor, whose job is to provide thermal stability for the transistor. Ce is the emitter by pass capacitors, which by-passes the amplified AC signals. If the emitter by-pass capacitor not there, the amplified ac voltages will drop across Re and it will get added on to the base-emitter voltage of Q1 and will disrupt the biasing conditions. Cin is the input DC decoupling capacitor while Cout is the output DC decoupling capacitor. The task of a DC decoupling capacitor is to prevent DC voltages from reaching the succeeding stage. Inductor L1, L2 and capacitor C1 forms the tank circuit.When the power supply is switched ON the transistor starts conducting and the collector current increases. As a result the capcitor C1 starts charging and when the capacitor C1 is fully charged it starts discharging through coil L1. This charging and discharging creates a series of damped oscillations in the tank circuit and it is the key.The oscillations produced in the tank circuit is coupled (fed back) to the base of Q1 and it appears in the amplified form across the collector and emitter of the transistor. The output voltage of the transistor (voltage across collector and emitter) will be in phase with the voltage across inductor L1. Since the junction of two inductors is grounded, the voltage across L2 will be 180° out of phase to that of the voltage across L1. The voltage across L2 is actually fed back to the base of Q1. From this we can see that, the feed back voltage is 180° out of phase with the transistor and also the transistor itself will create another 180° phase difference. So the total phase difference between input and output is 360° and it is very important condition for creating sustained oscillations.



PART C

111 (a) It is plotted between Vbe and Ib ,making Vce constant..The base emitter junction is forward biased,when the Vce increases the curve resembles like a diode.





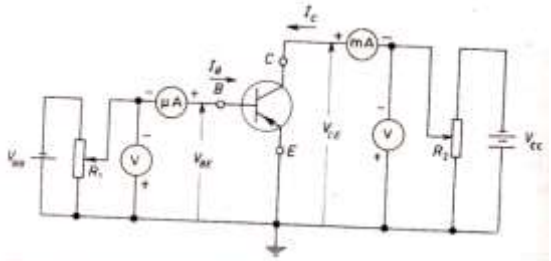


Fig. 5.17 Circuit arrangements for determining the static characteristics of a *PNP* transistor, in CE configuration

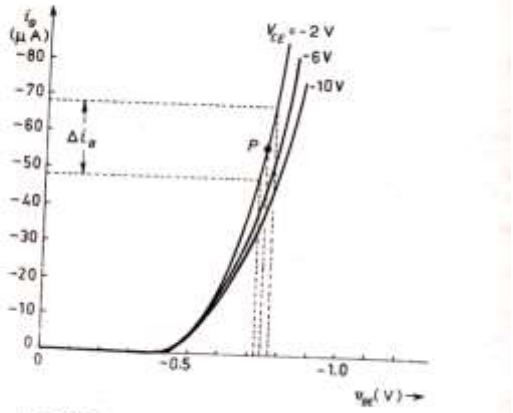


Fig. 5.18 Common-emitter input characteristics of a *PNP* transistor

. In active region,Ic slowly increases as Vce increases.

. Ic decreases rapidly when Vce decreases.At this condition the collector base junction is in forward biased .this is called saturation region

. In active region,the Ic is beta times greater than the Ib.so for small i/p current ,the Ib produces a large o/p current Ic.

.The Ic will not be zero when Ib is zero,there exists a small leakage current called Iceo

(b)

Ordinary Diode	Zener Diode
(*) Current conducts only in one direction	(*) Allows the conduction in both directions
(*) The diode will be permenently damaged for a large reverse current.	(*) It will not damage
(*) Diode are normally used for rectification	(*) Zener diode are used for voltage regulation.

1V

(a)

We know that, $I_E = I_C + I_B$ ... (1)

divide the above equation by I_C, we get

$$\frac{I_E}{I_C} = \frac{I_C}{I_C} + \frac{I_B}{I_C}$$

$$\frac{1}{\alpha} = 1 + \frac{1}{\beta}$$

$$\frac{1}{\beta} = \frac{1}{\alpha} - 1 = \frac{1-\alpha}{\alpha}$$

$$\therefore \quad \boxed{\beta = \frac{\alpha}{1-\alpha}} \qquad \text{... (2)}$$

from eq. (1), $I_B = I_E - I_C$

$$\therefore \quad \gamma = \frac{I_E}{I_B} = \frac{I_E}{I_E - I_C}$$

dividing the N.R and D.R on RHS by I_E, we get

$$\gamma = \frac{I_E/I_E}{\frac{I_E}{I_E} - \frac{I_C}{I_E}} = \frac{1}{1-\alpha}$$

$$\therefore \quad \boxed{\gamma = \frac{1}{1-\alpha}}$$

Adding 1 to eq. (2) on both sides, we get

$$\beta + 1 = \frac{\alpha}{1-\alpha} + 1 = \frac{\alpha + 1 - \alpha}{1-\alpha} = \frac{1}{1-\alpha} = \gamma$$

$$\therefore \quad \gamma = \beta + 1.$$

(b) The holes are repelled from the +ve terminal of the battery and are compelled to move towards the junction. Electrons repel led from –ve terminal of the battery and drift towards the junction. Due to its energy some electrons and holes will penetrate the depletion region. This reduces the potential barrier. Majority carriers diffuse across the junction. These carriers recombine and cause movement of charge carriers in the space charge region. For each recombination of free electron and hole that occurs, an electron from the –ve terminal of battery enters the N type material. It then drift towards the junction.The flow of carriers due to applied voltage is called drift current and whereas the current flows as a result of gradient of carrier concentration is called diffusion current.

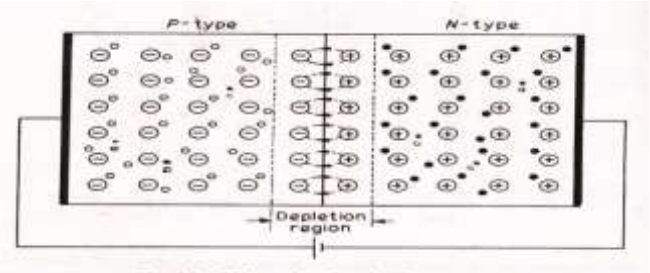
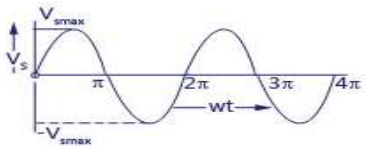
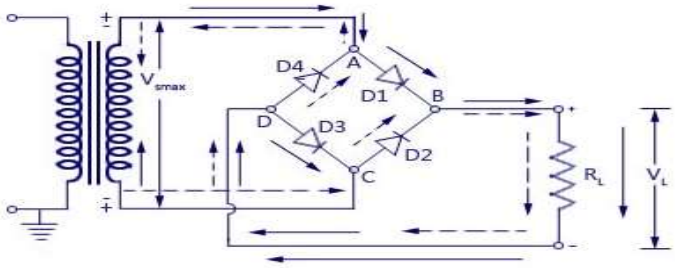


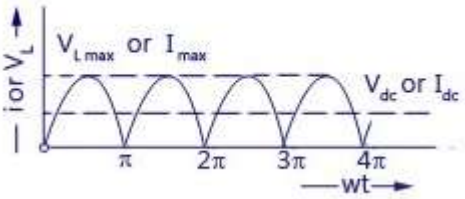
Fig. 4.3 *PN*-junction showing forward bias

V (a)



Input Voltage Waveform

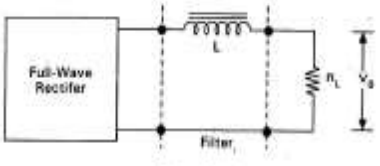


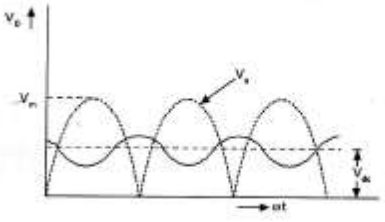


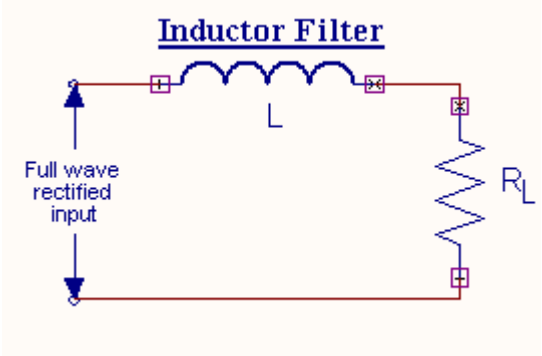
During first half cycle of the input voltage, the upper end of the transformer secondary winding is positive with respect to the lower end. Thus during the first half cycle diodes D1 and D_3 are forward biased and current flows through arm AB, enters the load resistance R_L, and returns back flowing through arm DC. During this half of each input cycle, the diodes D_2 and D_4 are reverse biased and current is not allowed to flow in arms AD and BC. The flow of current is indicated by solid arrows in the figure above. We have developed another diagram below to help you understand the current flow quickly. During second half cycle of the input voltage, the lower end of the transformer secondary winding is positive with respect to the upper end. Thus diodes D_2 and D_4 become forward biased and current flows through arm CB, enters the load resistance R_L, and returns back to the source flowing through arm DA. Flow of current has been shown by dotted arrows in the figure. Thus the direction of flow of current through the load resistance R_L remains the same during both half cycles of the input supply voltage

(a) As the name of the filter circuit suggests, the Inductor L is connected in series between the rectifier circuit and the load. The inductor carries the property of opposing the change in current that flows through it.In other words, the inductor offers high impedance to the ripples and no impedance to the desired dc components. Thus the ripple components will be eliminated. When the rectifier output current increases above a certain value, energy is stored in it in the form of a magnetic field and this energy is given up when the output current falls below the average value. Thus all the sudden changes in current that occurs in the circuit will be smoothened by placing the inductor in series between the rectifier and the load.The waveform below shows the use of inductor in the circuit.From the circuit, for zero frequency dc voltage, the choke resistance Ri in series with the load resistance RL forms a voltage divider circuit, and thus the dc voltage across the load is

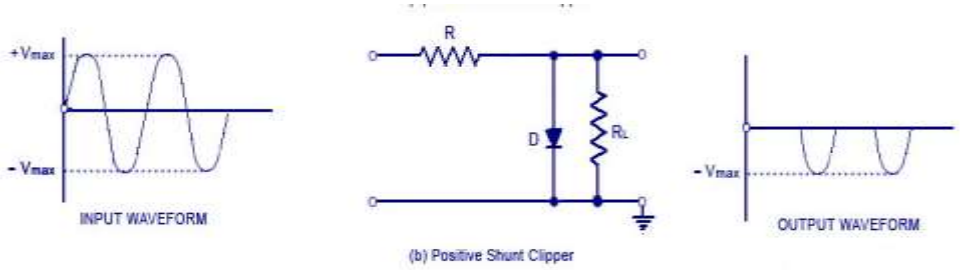
Vdc = RL/(Ri + RL)



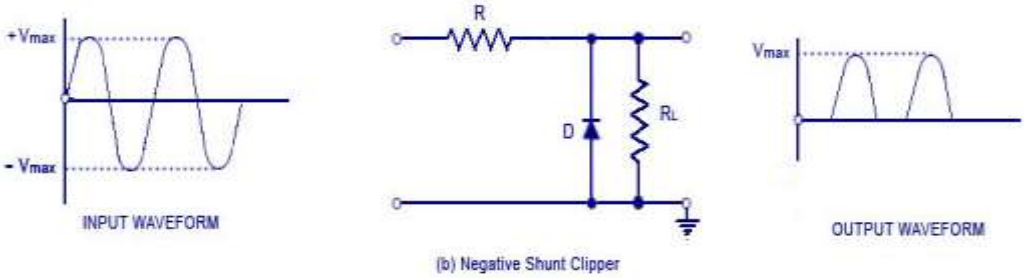




V1(a) During the positive half cycle, the diode 'D' is forward biased and the diode acts as a closed switch. This causes the diode to conduct heavily. This causes the voltage drop across the diode or across the load resistance R_L to be zero. Thus output voltage during the positive half cycles is zero, as shown in the output waveform. During the negative half cycles of the input signal voltage, the diode D is reverse biased and behaves as an open switch.



The negative clipping circuit is almost same as the positive clipping circuit, with only one difference. If the diode figures is reconnected with reversed polarity, the circuits will become for negative shunt clipper respectively.

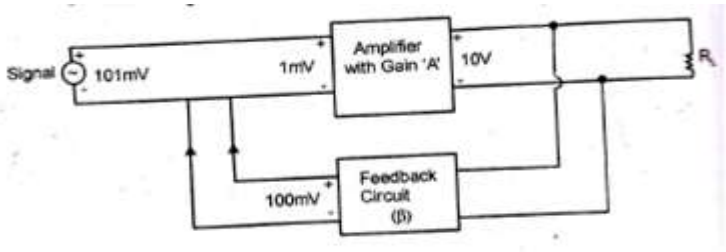


(b)

Characteristics	Half-wave Rectifier	Centre-tap Rectifier	Bridge Rectifier
1. No. of diodes	1	2	4
2. Need for centre-tapped transformer	No	Yes	No
3. Rectifier efficiency (max)	40.6%	81.2%	81.2%
4. Ripple factor	1.21	0.482	0.482
5. Ripple (or) output frequency (f_0)	f_{in}	$2 f_{in}$	$2 f_{in}$
6. Peak inverse voltage	V_m	$2V_m$	V_m
7. Rms current, (I_{rms})	$\frac{I_m}{2}$	$\frac{I_m}{\sqrt{2}}$	$\frac{I_m}{\sqrt{2}}$
8. Average or DC current, (I_{dc})	$\frac{I_m}{\pi}$	$\frac{2I_m}{\pi}$	$\frac{2I_m}{\pi}$

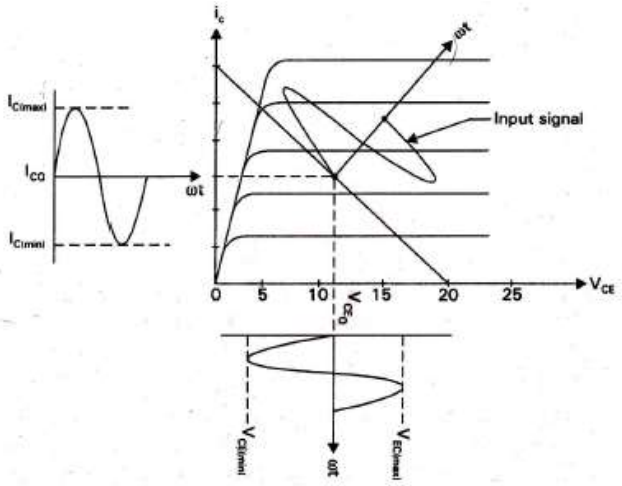
V11 (a) when any increase in the output signal results in a feedback signal into the input in such a way as to decrease the output signal the amplifier is said to have negative feedback.The output of the amplifier is 10v.The fraction beta of this output ie 100mV

is feedback to the input where it is applied in series with the input signal of 101mV.As the feedback is negative only 1mV appears At the input terminals of the amplifier.

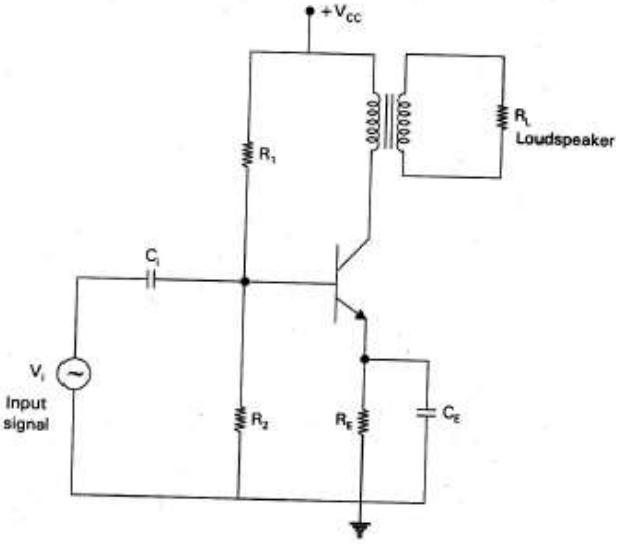


$$G = \frac{A}{1 + \beta A}$$

(a) It is also known as single-ended power amplifier (denoting only one transistor).The transistor is operated in class-A operating, the collector current flows for the complete cycle of the input signal. The circuit consists of an NPN transistor connected in CE configuration. Potential divider biasing is used with resistors RI, R2 and RE. The primary of the transformer is connected in series with the collector to the Vcc terminal. The load resistance (R_L is connected to the secondary of the transformer. Here, the transformer provides impedance matching.



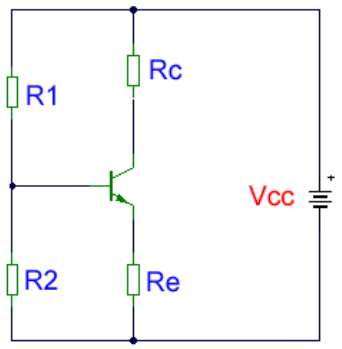
$$= \frac{V_{CE(Peak)}}{\sqrt{2}} \times \frac{I_{C(Peak)}}{\sqrt{2}}$$



It match the loudspeaker resistance (i.e., R_L) to the output resistance of the amplifier, to achieve maximum possible power output.The operating point is so selected that the transistor works only in the linear portion of its characteristics. This enables the circuit to produce maximum equal positive and negative changes in V. The input signal varies the base current. This variation in base current and the corresponding variations in collector current and collertor voltage are shown. The variation of collector voltage appears across the primary of the transformer. An a.c. voltage is induced in the secondary, which in turn develops ac power in R_L. From the graph the maximum and minimum values of the collector current and voltage are noted. The ac power developed across the transformer primary can be calculated to be the same power across the $R_{L,}$ if the transformer is 100% efficient

V111

(a)



Here R1 and R2 form a potential divider, which will fix the base potential of the transistor. The current through this bias chain is usually set at 10 times greater than the base current required by the transistor. The base emitter voltage drop of the transistor is approximated as 0.6 volt. There will also be a voltage drop across the emitter resistor, Re, this is generally set to about 10% of the supply voltage. The inclusion of this resistor also helps to stabilize the bias: If the temperature increases, then extra collector current will flow. If Ic increases, then so will Ie as Ie= Ib + Ic. The extra current flow through Re increases the voltage drop across this resistor reducing the effective base emitter voltage and therefore stabilizing the collector current. The equations follow:

Rc = Vc / Ic

Ie = Ib + Ic as Ic >> Ib then Ie ~ Ic

Ve = 10% * Vcc

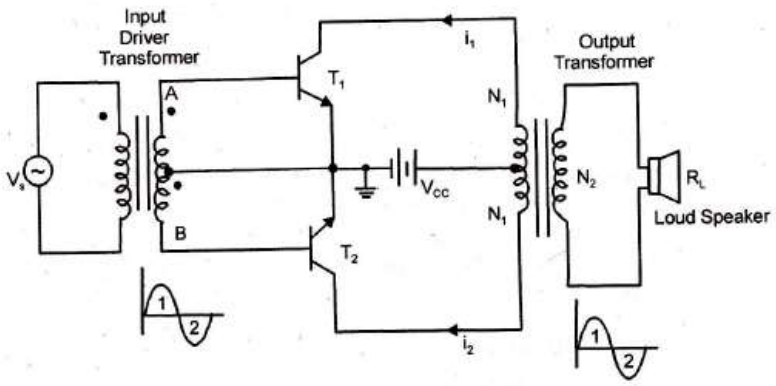
Re= Ve / Ie

Vb = Ve + 0.6

R2 = Vb / 10 * Ib

R1 = Vcc-Vb / 10 * Ib

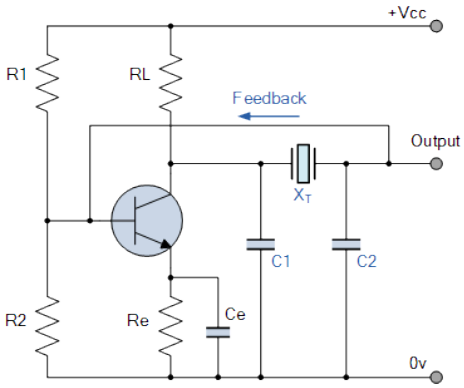
(b)

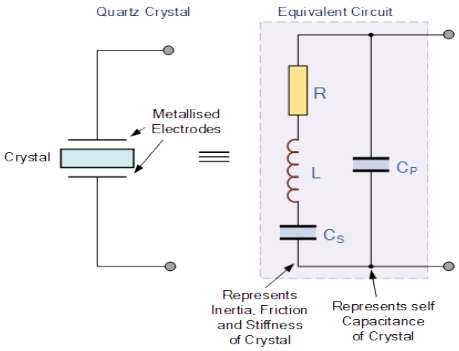


The input signal appears across the secondary AB of driver transformer. During the positive half cycle of the signal, end A becomes positive and end B negative. This will make the base - emitter junction of T, forward biased and that of T, reverse biased. The circuit will conduct current due to T, only, and is shown by current i,. Therefore, this half-cycle of the signal is amplified by T, and appears in the upper half of the primary of output transformer. During the negative half - cycle of the input signal, T2 is forward biased whereas T, is reverse biased. Therefore, T2 conducts and is shown by current i2. So, this half - cycle of the signal is amplified by T2 and appears in the lower half of the output transformer primary. The centre tapped primary of the output transformer combines two collector currents to form a sine wave output in the secondary. Thus the two transistors conduct in alternate half cycles of the input signal. Hence the collector current flow in opposite direction. So the net d.c in the primary is zero. However, the secondary of the output transformer will have induced voltage. Output of the amplifier will be twice that of the output offered by the single transistor. The push - pull arrangement also permits a maximum transfer of power to the load through impedance matching. The turns ratio 2 N, : N2 of the transformer is chosen so that the load R_L is matched with the output impedance of the transistor. If R_L is the resistance connected across the secondary of output transformer, then the resistance looking into the primary is

$$R_L^1 = \left(\frac{2N_1}{N_2}\right)^2 R_L$$

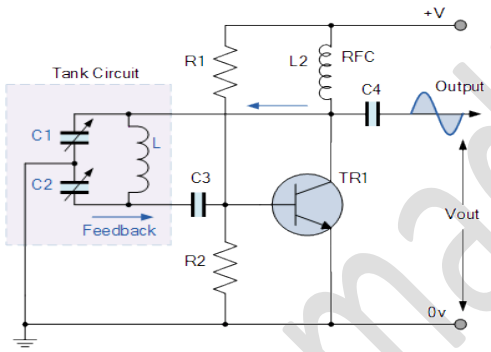
1X (a) These types of **Crystal Oscillators** are designed around the common emitter amplifier stage of a **Colpitts Oscillator**. The input signal to the base of the transistor is inverted at the transistors output. The output signal at the collector is then taken through a 180^o phase shifting network which includes the crystal operating in a series resonant mode.The output is also fed back to the input which is “in-phase” with the input providing the necessary positive feedback. Resistors, R1 and R2 bias the resistor in a Class A type operation while resistor Re is chosen so that the loop gain is slightly greater than unity.





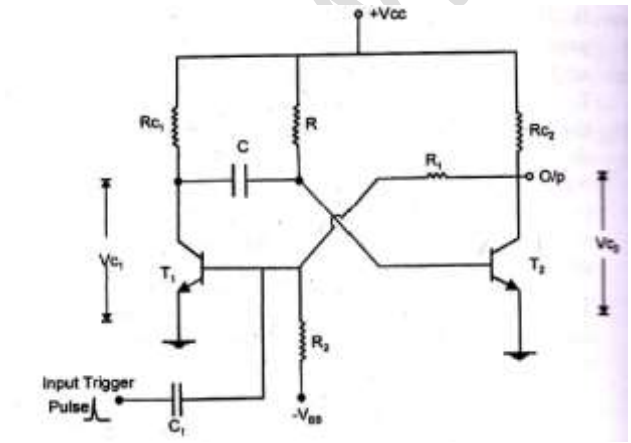
Capacitors, C1 and C2 are made as large as possible in order that the frequency of oscillations can approximate to the series resonant mode of the crystal and is not dependent upon the values of these capacitors.The circuit diagram above of the **Colpitts Crystal Oscillator** circuit shows that capacitors, C1 and C2 shunt the output of the transistor which reduces the feedback signal. Therefore, the gain of the transistor limits the maximum values of C1 and C2. The output amplitude should be kept low in order to avoid excessive power dissipation in the crystal otherwise could destroy itself by excessive vibration.

(b) The transistor amplifiers emitter is connected to the junction of capacitors, C1 and C2 which are connected in series and act as a simple voltage divider. When the power supply is firstly applied, capacitors C1 and C2 charge up and then discharge through the coil L. The oscillations across the capacitors are applied to the base-emitter junction and appear in the amplified at the collector output.The amount of feedback depends on the values of C1 and C2 with the smaller the values of C the greater will be the feedback.The required external phase shift is obtained in a similar manner to that in the Hartley oscillator circuit with the required positive feedback obtained for sustained un-damped oscillations. The amount of feedback is determined by the ratio of C1 and C2. These two capacitances are generally "ganged" together to provide a constant amount of feedback so that as one is adjusted the other automatically follows.



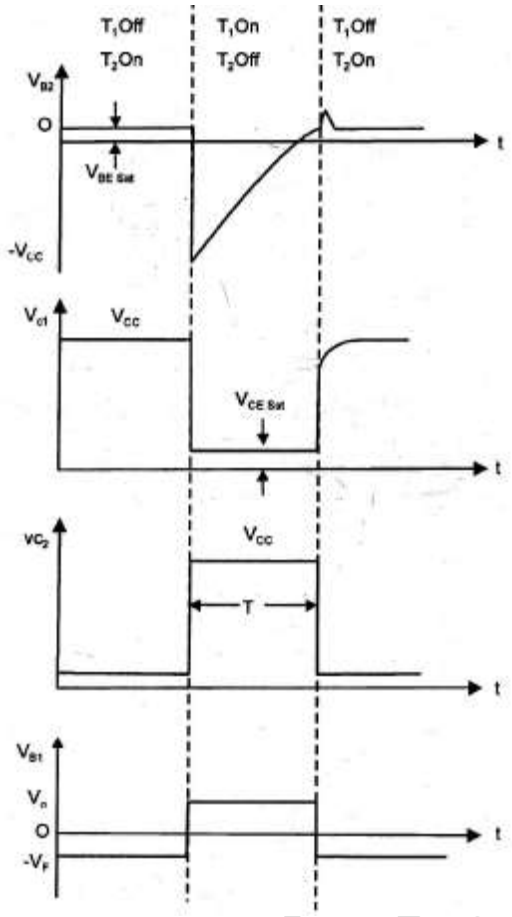
X

(a)

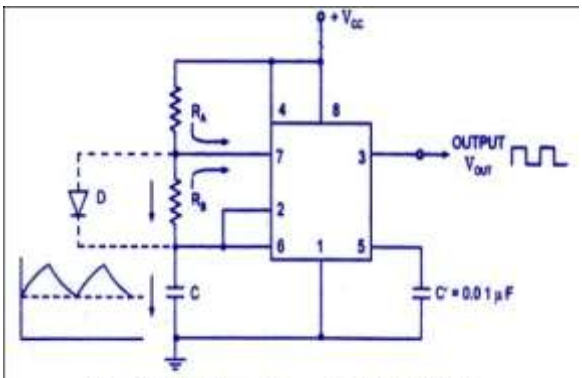


The negative supply voltage $-V_{BB}$ in conjunction with resistors R1 and R2 keeps the transistor T1 OFF_ Hence T2 conducts at saturation i.e., it is ON. This constitutes the state of the multivibrator. The initial stable state is represented by (i) T1 is at cut off and (ii) T2 is at saturation The circuit will continue to stay in this state until triggering pulse is applied at C1. When a positive trigger pulse of sufficient amplitu is applied to the base of T1 through C1, the transistor T1 starts conducting. As T1 conducts, its collector voltage falls due to voltage drop across R_{c1}. This negative going voltage at the collector of T1 is coupled to the base of

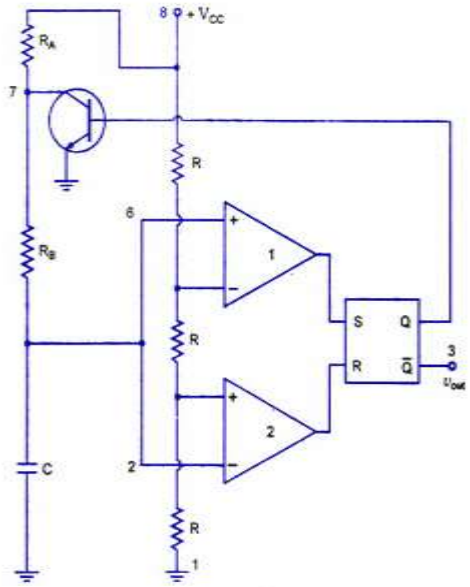
T2 through capacitor C. This decreases the forward bias on T2 and its collector current decreases. As collector current of T2 starts decreasing, the collector voltage of T2 increases and is coupled to the base of T1 through RI. This further increases the forward bias on T1 and hence its collector current. This action is cumulative and ends with TI conducting at saturation and T2 cutoff. The circuit stays in this quasi-stable state for only finite time T because base of T2 is connected to supply voltage Vcc through the resistor R. Capacitor C now begins to discharge through the transistor T1 This decreases the reverse bias on the base of T2 Ultimately, the base of T2 becomes forward biased_ Now T2 begins to conduct. It drives the transistor T1 towards cutoff. A regenerative action begins which ultimately turns T1 OFF and T2 ON returning the multivibrator to its original stable state. It remains in this state till another trigger pulse causes the circuit to change the states. Since this multivibrator produces one output pulse for every input trigger pulse, it is called mono (or) one-shot multivibrator-The width or duration of the pulse is given by T= 0.693 RC



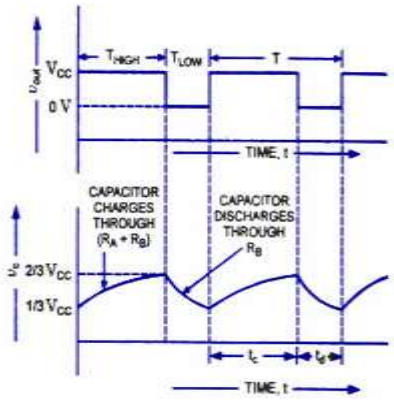
(b) when Q is low or output V_{OUT} is high, the discharging transistor is cut-off and the capacitor C begins charging toward V_{CC} through resistances R_A and R_B. Because of this, the charging time constant is $(R_A + R_B)$ C. Eventually, the threshold voltage exceeds +2/3 V_{CC}, the comparator 1 has a high output and triggers the flip-flop so that its Q is high and the timer output is low. With Q high, the discharge transistor saturates and pin 7 grounds so that the capacitor C discharges through resistance R_B with a discharging time constant R_B C. With the discharging of capacitor, trigger voltage at inverting input of comparator 2 decreases. When it drops below $1/3V_{CC}$, the output of comparator 2 goes high and this reset the flip-flop so that Q is low and the timer output is high. This proves the auto-transition in output from low to high and then to low as, illustrated in fig ures. Thus the cycle repeats.



Circuit of The Timer 555 as an Astable Multivibrator



Internal Circuitry With External Connections



Capacitor and Output Voltage Waveforms

Astable Operation