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THIRD SEMESTER DIPLOMA EXAMINATION IN ELECTRICAL & ELECTRONICS ENGINEERING, OCTOBER 2012

ELECTRONIC DEVICES AND CIRCUITS

Time :3hours Maximum marks:100

PART A (maximum marks 10)

I. Answer the following questions in 2 or 3 sentences:

1A the charge carriers have the tendency to move from the region of higher concentration to that of lower concentration of the same type of charge carriers. Thus the movement of charge carriers takes place resulting in a current called diffusion current.

2A The **Zener breakdown** is a type of electrical breakdown in a reverse biased p-n diode in which the electric field enables tunneling of electrons from the valence to the conduction band of a semiconductor, leading to a large number of free minority carriers, which suddenly increase the reverse current.

3A It is the maximum value of *reverse voltage* which occurs at the *peak* of the input cycle when the diode is *reverse*-biased.

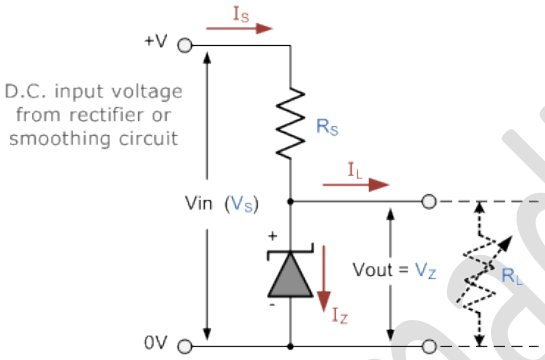
4A Bandwidth can be defined as range of frequencies over which the gain is equal to or greater than 0.707 .the frequencies at which the voltage gain reduces to 0.707 of the maximum gain are known as cut off frequencies of the amplifier.

5A Circuit which produces electrical oscillations of any desired frequency is called tank circuit

PART B (Maximum marks :30)

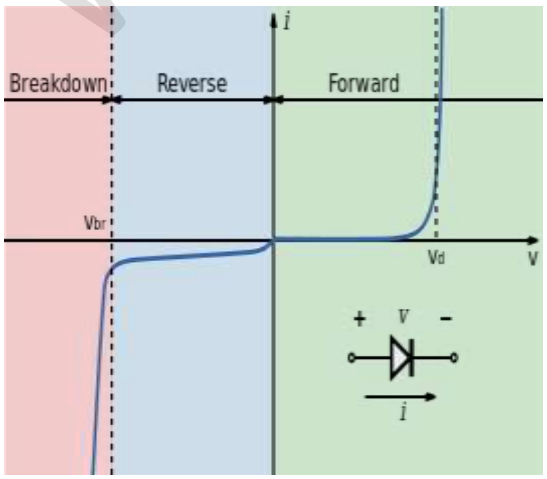
II Answer any five questions from the following

1A



The resistor, R_S is connected in series with the zener diode to limit the current flow through the diode with the voltage source, V_S being connected across the combination. The stabilised output voltage V_{out} is taken from across the zener diode. The zener diode is connected with its cathode terminal connected to the positive rail of the DC supply so it is reverse biased and will be operating in its breakdown condition. Resistor R_S is selected so to limit the maximum current flowing in the circuit.With no load connected to the circuit, the load current will be zero, ($I_L = 0$), and all the circuit current passes through the zener diode which in turn dissipates its maximum power. Also a small value of the series resistor R_S will result in a greater diode current when the load resistance R_L is connected and large as this will increase the power dissipation requirement of the diode so care must be taken when selecting the appropriate value of series resistance so that the zener's maximum power rating is not exceeded under this no-load or high-impedance condition.The load is connected in parallel with the zener diode, so the voltage across R_L is always the same as the zener voltage, ($V_R = V_Z$). There is a minimum zener current for which the stabilization of the voltage is effective and the zener current must stay above this value operating under load within its breakdown region at all times. The upper limit of current is of course dependant upon the power rating of the device. The supply voltage V_S must be greater than V_Z.

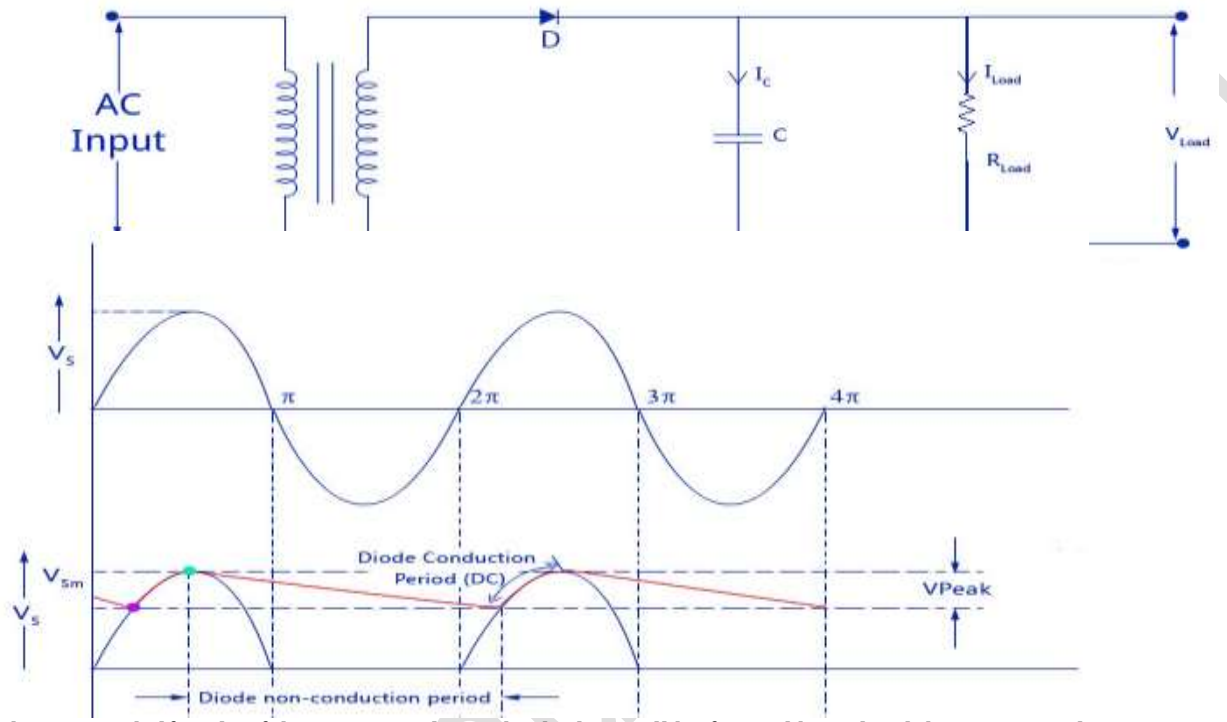
2A



Forward: The Vaa is connected to the diode via potentiometer P.current flows through fwd biased diode, resistance R is used to limit the current flow The diode does not conduct until the external voltage overcomes the barrier potential. When reaches 0.7V large no. of free electrons and holes will cross the junction.Above0.7V even a small increase in voltage produces a large increase in current. The voltage at which the current starts to increase rapidly is called knee voltage or cut in voltage Si=0.7V
Ge=0.3V

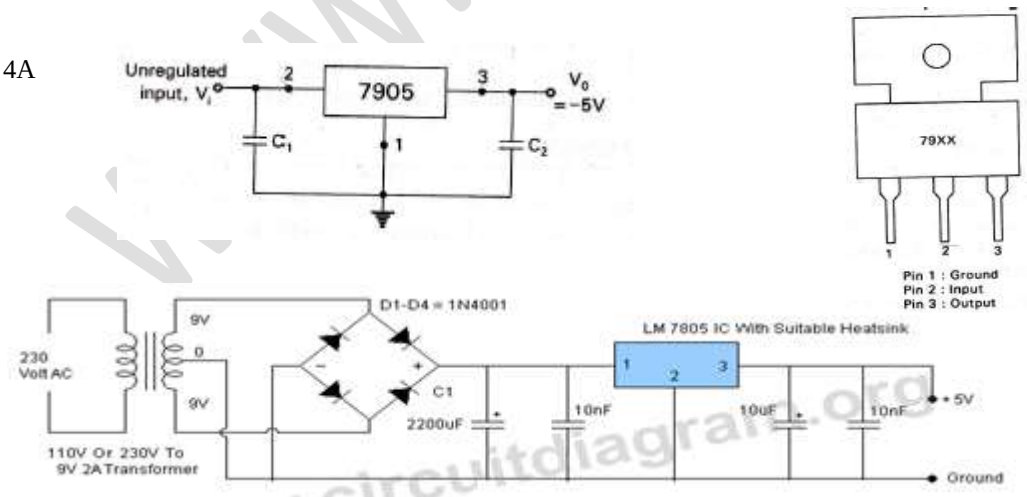
Reverse bias characteristics: The diode current is very small. It remains small and almost constant for all voltages less than the breakdown voltage Vz.At breakdown the voltage increases rapidly for small increase in voltage.

3A



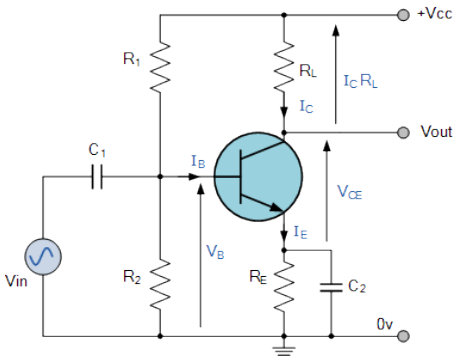
During the positive half cycle of the input ac voltage, the diode D will be forward biased and thus starts conducting. During this period, the capacitor 'C' starts charging to the maximum value of the supply voltage Vsm. When the capacitor is fully charged, it holds the charge until the input ac supply to the rectifier reaches the negative half cycle. As soon as the negative half supply is reached, the diode gets reverse biased and thus stops conducting. During the non-conducting period, the capacitor 'C' discharges all the stored charges through the output load resistance RLoad. As the voltage across RLoad and the voltage across the capacitor 'C' are the same (VLoad = Vc), they decrease exponentially with a time constant (C*RLoad) along the curve of the non-conducting period.

4A



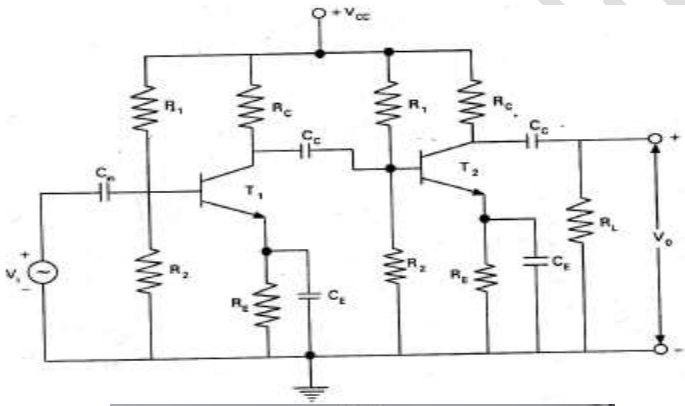
pin 2 is the input terminal, pin 1 is the ground and pin 3 is the output terminal. The unregulated input voltage (V1) is given to the input terminal. The output is taken from the output terminal. Filter capacitors are shown to be connected at the input and output side. The input capacitor C1 is used to cancel the inductive effects due to long distiibution leads and the output capacitor C2 improves the transient response.

5A

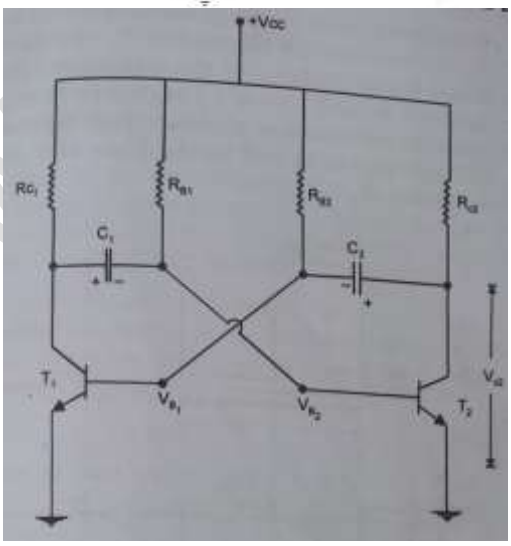


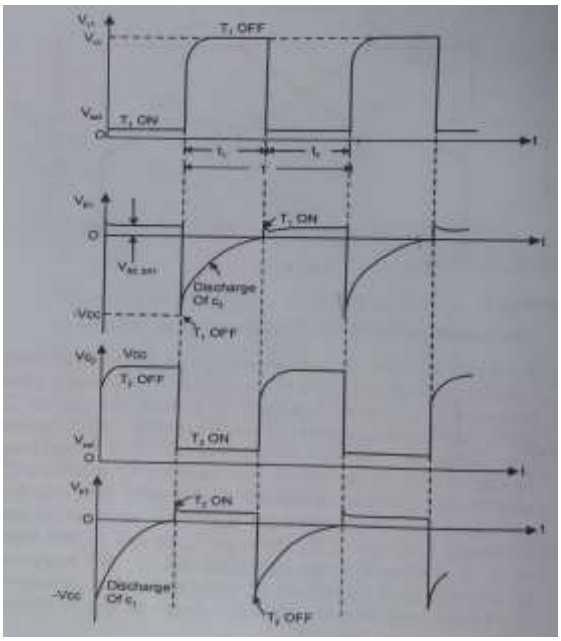
In **Common Emitter Amplifier** circuits, capacitors C1 and C2 are used as **Coupling Capacitors** to separate the AC signals from the DC biasing voltage. the capacitors will only pass AC signals and block any DC component. The output AC signal is then superimposed on the biasing of the following stages. Also a bypass capacitor, C_E is included in the Emitter leg circuit.This capacitor is an open circuit component for DC bias meaning that the biasing currents and voltages are not affected by the addition of the capacitor maintaining a good Q-point stability. However, this bypass capacitor short circuits the Emitter resistor at high frequency signals and only R_L plus a very small internal resistance acts as the transistors load increasing the voltage gain to its maximum. Generally, the value of the bypass capacitor, C_E is chosen to provide a reactance of at most, 1/10th the value of R_E at the lowest operating signal frequency.

6A When an ac signal is applied to the input of first stage, it gets amplified by this stage and appears across the collector resistor itc of first-stage: This output voltage of first-stage is coupled to the base of the second stage through the coupling capacitor C. The amplified signal of first stage gets further amplification by the second stage and hence more amplification takes place. The output of the stage is taken out through the coupling the overall gain of amplification is equal so product of the individual stage gains. Av = Av1 * Av2 It Is to be noted that as the configuration employed Is CE configuration, each stage of amplification produces a phase shift of the input signal by 180. The overall phase shift is 2 x 180,or 360° or there's no phase difference between the input signal and the output of the second stage of amplification



7A





Because of circuit variations, one transistor will conduct heavily than the other. Assume that transistor T1 starts conducting before. transistor T2 does. Its collector current rises rapidly. This causes its collector voltage to decrease. The resulting negative signal is fed to the base of T2 through C1 and drives it towards cutoff. As a result, the collector voltage of T2 rises towards Vcc. The increase in the collector voltage of T2 through C2 is fed to the base of T1 . It causes T1 to go into saturation. This happens SO quickly that capacitor C1 does not get a chance to discharge and the decreased voltage at the collector of T1 appears across RB1

The off time for transistor T_2 is t_2

$$t_2 = 0.693\ R_{B1}\ C_1$$

The off time for transistor T_1 is t_1

$$t_1 = 0.693\ R_{B2}\ C_2$$

$\therefore$ Total period, $T = t_1 + t_2 = 0.693\ (R_{B1}\ C_1 + R_{B2}\ C_2)$

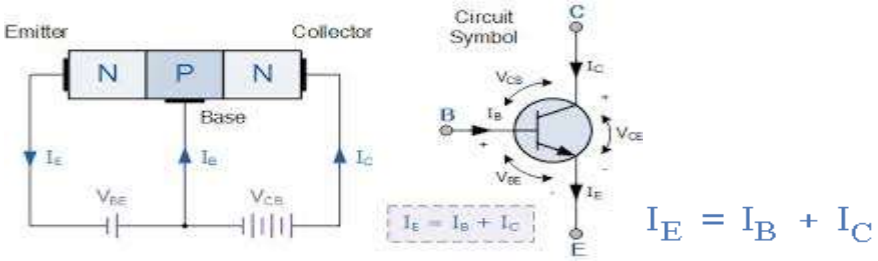
For a symmetric circuit with $R_{B1} = R_{B2} = R$ and $C_1 = C_2 = C$, we have

$$T = 1.386\ RC, \text{ seconds.}$$

and $$f = \frac{1}{T} = \frac{1}{1.386\,RC}\ \text{Hz.}$$

PART C

111 (a) Potential is applied across the base/emitter junction this makes the base/emitter junction forward biased.A much higher potential is applied across the base/collector junction with a relatively high positive voltage applied to the collector, so that the base/collector junction is heavily reverse biased. This makes the depletion layer between base and collector . When the base emitter junction is forward biased, a small current will flow into the base. Therefore holes are injected into the P type material. These holes attract electrons across the forward biased base/emitter junction to combine with the holes.Because the emitter region is very heavily doped, many more electrons cross into the base region than are able to combine with holes. This means there is a large concentration of electrons in the base region and most of these electrons are swept straight through the very thin base and enters in to the collector material.Varying the current flowing into the base, affects the number of electrons attracted from the emitter. In this way very small changes in base current cause very large changes in the current flowing from emitter to collector, so current amplification is taking place.



$$I_E = I_B + I_C$$

(a)

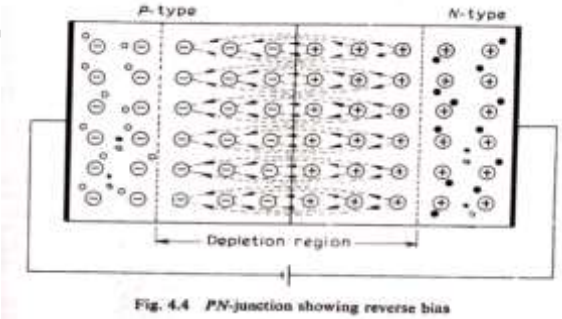


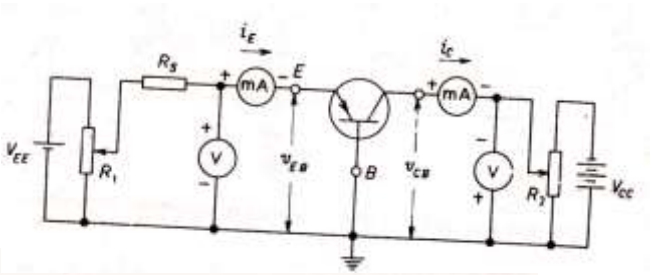
Fig. 4.4 *PN*-junction showing reverse bias

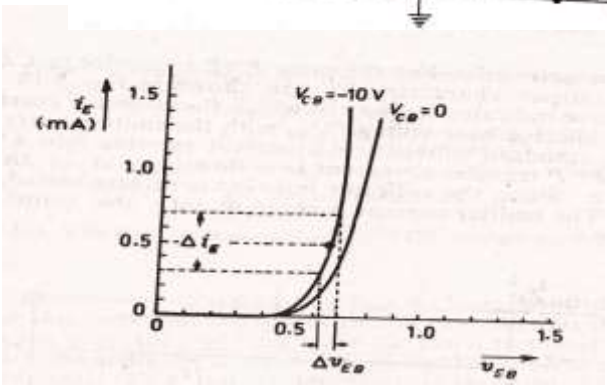
In p type the majority charge carriers are holes and in N type it is electrons.The p type semiconductor is attached to a negative terminal of the battery and n type semiconductor is attached to a positive terminal of the battery. if a reverse biasing potential is applied across these semiconductors then the holes and electrons are attracted to the terminal there by increasing the depletion

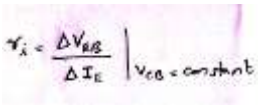
region width. So the majority charge carriers will move away from the junction, hence the minority charge carriers will cause a small current while crossing the junction.

IV (a) **common base configuration :** It is plotted between Veb and Ie ,making Vcb constant..The emitter base junction is forward biased,when the Vcb increases the curve resembles like a diode.

Input



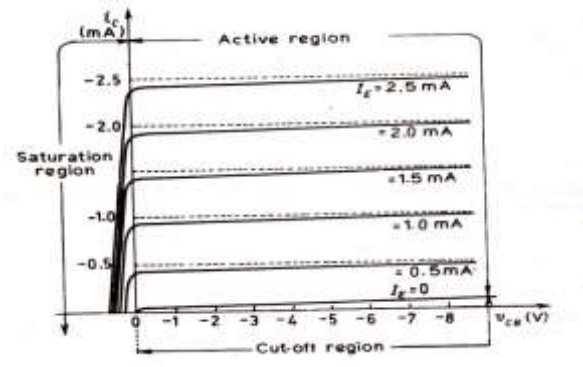




Output characteristics of common base (CB): The collector current Ic is approximately equal to the emitter current Ie

.In active region ,the curve are almost flat.This shows that Ic increases only slightly as Vcbinctreases.

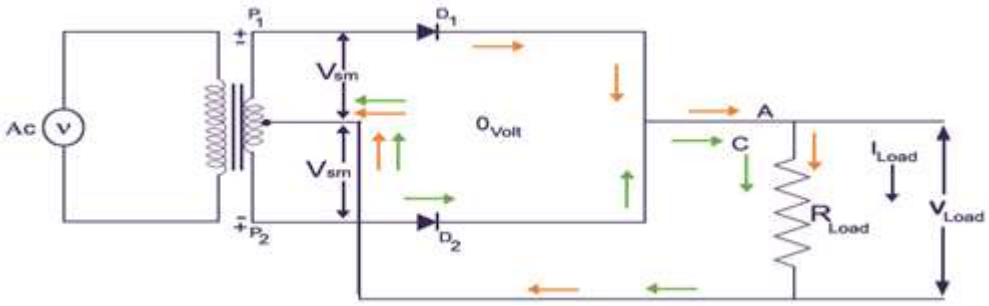
.As Vcb becomes +ve the collector current Ic sharply decreases.This is the saturation region.In this region the collector doesnot depend much upon the emitter current..

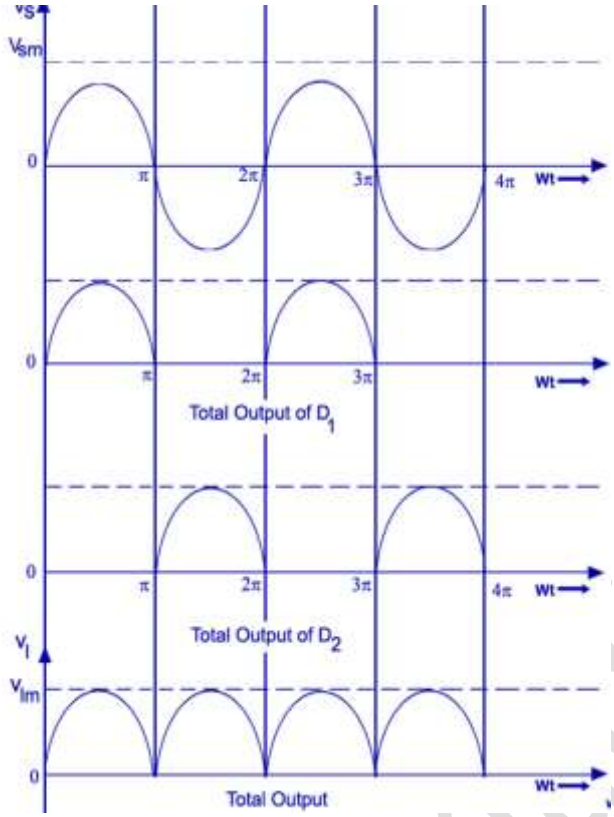


.The collector current is not zero when Ie=0.It has a small value.This is the reverse leackage current Ico

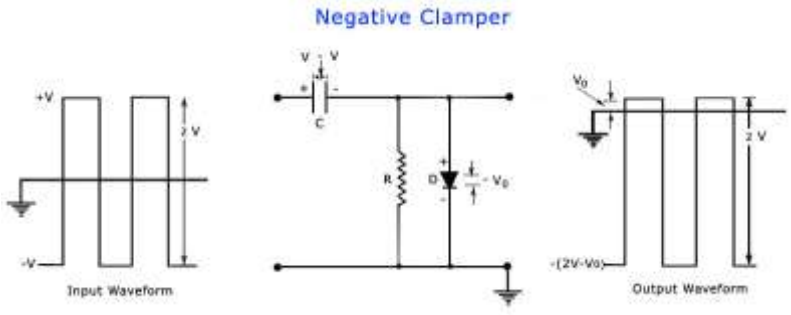
(a) Clipper,clamper,regulator,rectifier,switching,detection.

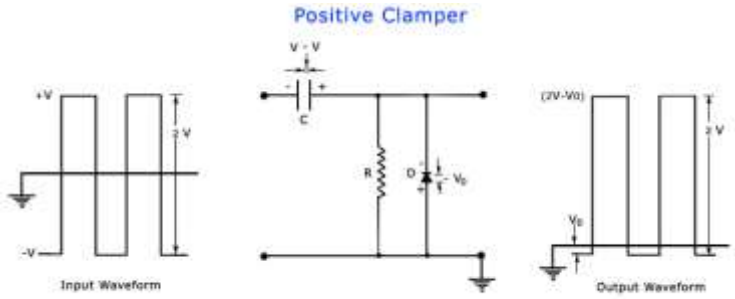
V (a) This input makes the secondary ends P1 and P2 become positive and negative alternately. For the positive half of the ac signal, the secondary point D1 is positive, GND point will have zero volt and P2 will be negative. At this instant diode D1 will be forward biased and diode D2 will be reverse biased. As explained in the Theory Behind P-N Junction and Characteristics of P-N Junction Diode, the diode D1 will conduct and D2 will not conduct during during the positive half cycle. Thus the current flow will be in the direction P1-D1-C-A-B-GND. Thus, the positive half cycle appears across the load resistance RLOAD.During the negative half cycle, the secondary ends P1 becomes negative and P2 becomes positive. At this instant, the diode D1 will be negative and D2 will be positive with the zero reference point being the ground, GND. Thus, the diode D2 will be forward biased and D1 will be reverse biased. The diode D2 will conduct and D1 will not conduct during the negative half cycle. The current flow will be in the direction P2-D2-C-A-B-GND.



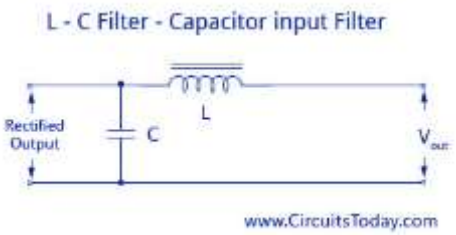


(a) The circuit will be called a positive clamper , when the signal is pushed upward by the circuit. When the signal moves upward, the negative peak of the signal coincides with the zero level.The circuit will be called a negative clamper, when the signal is pushed downward by the circuit. When the signal is pushed on the negative side the positive peak of the input signal coincides with the zero level. The diode D will be forward biased and the capacitor C is charged with the polarity shown, when an input signal is applied. During the positive half cycle of input, the output voltage will be equal to the barrier potential of the diode, V_0 and the capacitor is charged to $(V - V_Q)$. During the negative half cycle, the diode becomes reverse-biased and acts as an open-circuit. Thus, there will be no effect on the capacitor voltage. The resistance R, being of very high value, cannot discharge C a lot during the negative portion of the input waveform. Thus during negative input, the output voltage will be the sum of the input voltage and the capacitor voltage and is equal to $– V – (V — V_0)$ or $– (2 V – V_0)$. The value of the peak-to-peak output will be the difference of the negative and positive peak voltage levels is equal to V_0-[-(2V-V_0)] or 2 V.

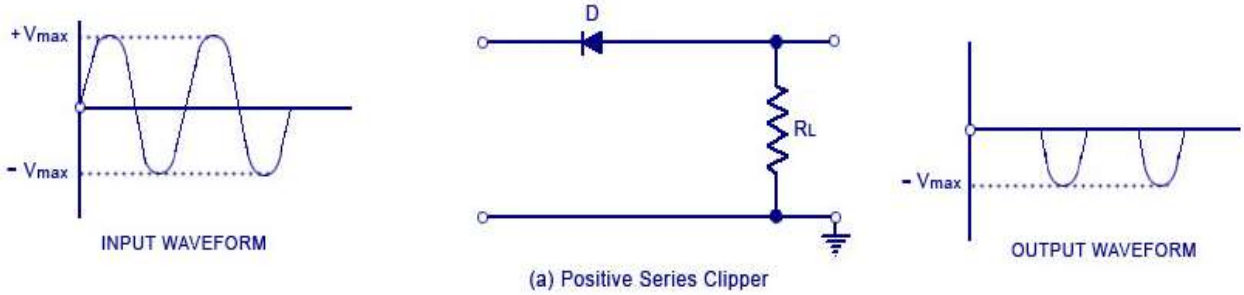




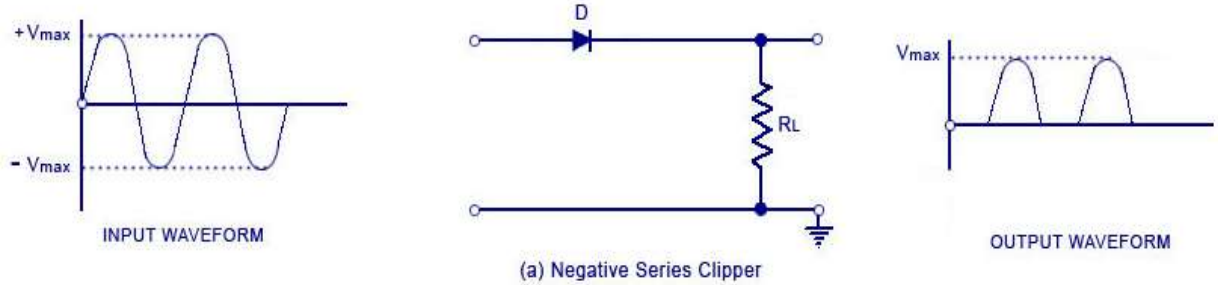
VI (a) The name pi – Filter implies to the resemblance of the circuit to a Π shape with two shunt capacitances (C1 and C2) and an inductance filter 'L'. As the rectifier output is provided directly into the capacitor it also called a capacitor input filter.The output from the rectifier is first given to the shunt capacitor C. The rectifier used can be half or full wave and the capacitors are usually electrolytic even though they large in size. In practical applications, the two capacitances are enclosed in a metal container which acts as a common ground for the two capacitors. The Π – Filter has some advantages like higher dc voltage and smaller ripple factor. But it also has some disadvantages like poor voltage regulation, high peak diode current, and high peak inverse voltage.This filter is divided into two – a capacitor filter and a L-section filter. The capacitor C1 does most of the filtering in the circuit and the remaining ripple os removed by the L-section filter (L-C2). C1 is selected to provide very low reactance to the ripple frequency. The voltage regulation is poor for this circuit as the output voltage falls off rapidly with the increase in load current.



(b)



During the positive half cycle of the input waveform, the diode 'D' is reverse biased, which maintains the output voltage at 0 Volts. Thus causes the positive half cycle to be clipped off. During the negative half cycle of the input, the diode is forward biased and so the negative half cycle appears across the output.



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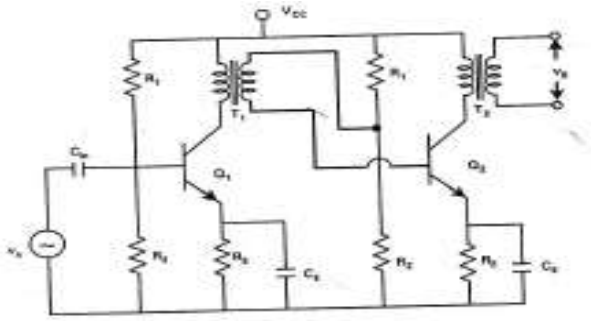
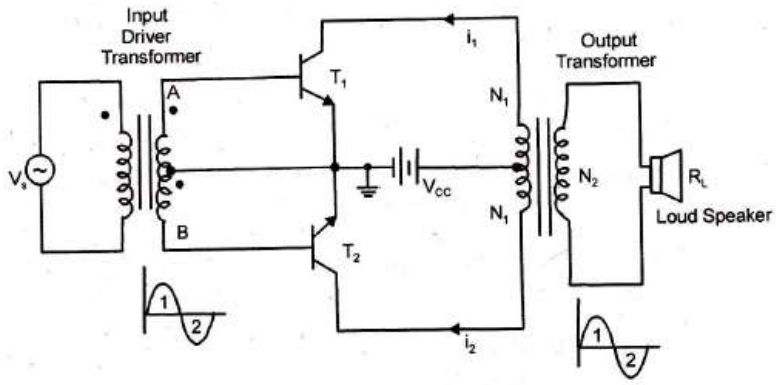
VII (a)



The input ac signal is applied to the base of the first stage transistor. It is amplified by the first stage and appears across the primary winding of the transformer T,. The amplified ac voltage across the primary winding of T, is transferred to the secondary winding,by induction and is given to the input of the second stage. It ls further amplified by the second stage amplifier. The output appears across the secondary winding of transformer, T2

(b)

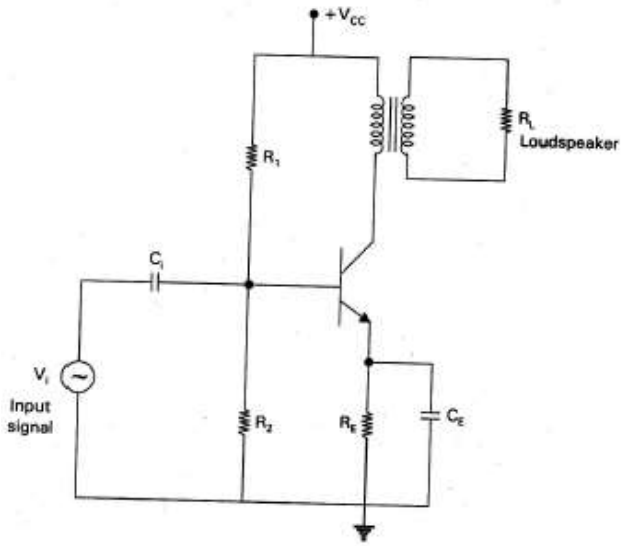


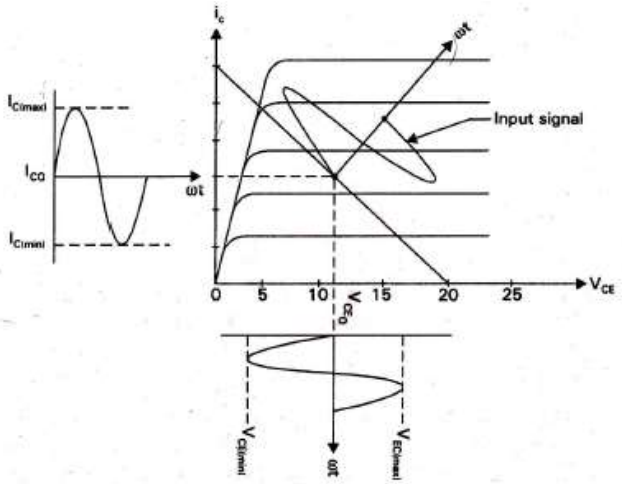
The input signal appears across the secondary AB of driver transformer. During the positive half cycle of the signal, end A becomes positive and end B negative. This will make the base - emitter junction of T, forward biased and that of T, reverse biased. The circuit will conduct current due to T, only, and is shown by current i,. Therefore, this half-cycle of the signal is amplified by T, and appears in the upper half of the primary of output transformer. During the negative half - cycle of the input signal, T2 is forward biased whereas T, is reverse biased. Therefore, T2 conducts and is shown by current i2. So, this half - cycle of the signal is amplified by T2 and appears in the lower half of the output transformer primary. The centre tapped primary of the output transformer combines two collector currents to form a sine wave output in the secondary. Thus the two transistors conduct in alternate half cycles of the input signal. Hence the collector current flow in opposite direction. So the net d.c in the primary is zero. However, the secondary of the output transformer will have induced voltage. Output of the amplifier will be twice that of the output offered by the single transistor. The push - pull arrangement also permits a maximum transfer of power to the load through impedance matching. The turns ratio 2 N, : N2 of the transformer is chosen so that the load R_L is matched with the output impedance of the transistor. If R_L is the resistance connected across the secondary of output transformer, then the resistance looking into the primary is

$$R_L^1 = \left(\frac{2N_1}{N_2}\right)^2 R_L$$

VIII (a) Direct coupling, inductor coupling,RC coupling, Transformer coupling

(a)



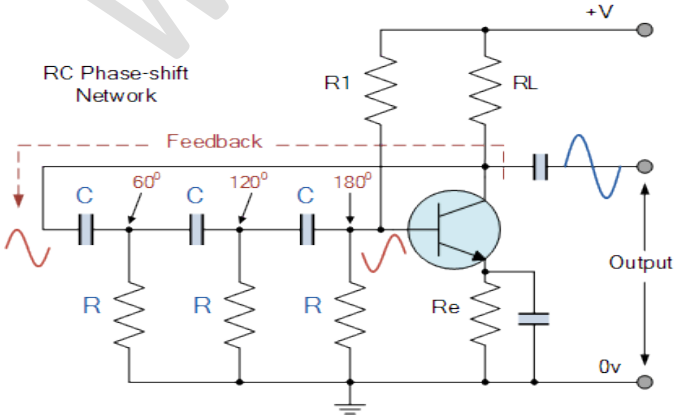


$$P_{0(ac)} = V_{CE\,(rms)} \times I_{C(rms)}$$

$$= \frac{V_{CE(Peak)}}{\sqrt{2}} \times \frac{I_{C(Peak)}}{\sqrt{2}}$$

It is also known as single-ended power amplifier (denoting only one transistor).The transistor is operated in class-A operating, the collector current flows for the complete cycle of the input signal. The circuit consists of an NPN transistor connected in CE configuration. Potential divider biasing is used with resistors RI, R2 and RE. The primary of the transformer is connected in series with the collector to the Vcc terminal. The load resistance (R_L is connected to the secondary of the transformer. Here, the transformer provides impedance matching. It match the loudspeaker resistance (i.e., R_L) to the output resistance of the amplifier, to achieve maximum possible power output.The operating point is so selected that the transistor works only in the linear portion of its characteristics. This enables the circuit to produce maximum equal positive and negative changes in V. The input signal varies the base current. This variation in base current and the corresponding variations in collector current and collertor voltage are shown. The variation of collector voltage appears across the primary of the transformer. An a.c. voltage is induced in the secondary, which in turn develops ac power in R_L. From the graph the maximum and minimum values of the collector current and voltage are noted. The ac power developed across the transformer primary can be calculated to be the same power across the $R_{L,}$ if the transformer is 100% efficient

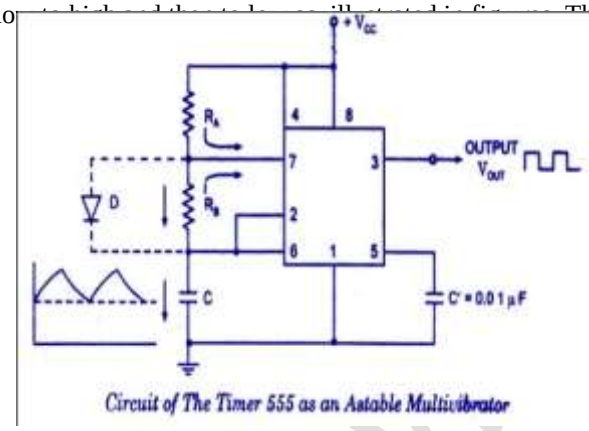
IX (a) The basic **RC Oscillator** which is also known as a **Phase-shift Oscillator**, produces a sine wave output signal using regenerative feedback obtained from the resistor-capacitor combination. This regenerative feedback from the RC network is due to the ability of the capacitor to store an electric charge, (similar to the LC tank circuit).This resistor-capacitor feedback network can be connected as shown above to produce a leading phase shift (phase advance network) or interchanged to produce a lagging phase shift (phase retard network) the outcome is still the same as the sine wave oscillations only occur at the frequency at which the overall phase-shift is 360^o.By varying one or more of the resistors or capacitors in the phase-shift network, the frequency can be varied and generally this is done by keeping the resistors the same and using a 3-ganged variable capacitor.If all the resistors, R and the capacitors, C in the phase shift network are equal in value, then the frequency of oscillations produced by the RC oscillator is given as:



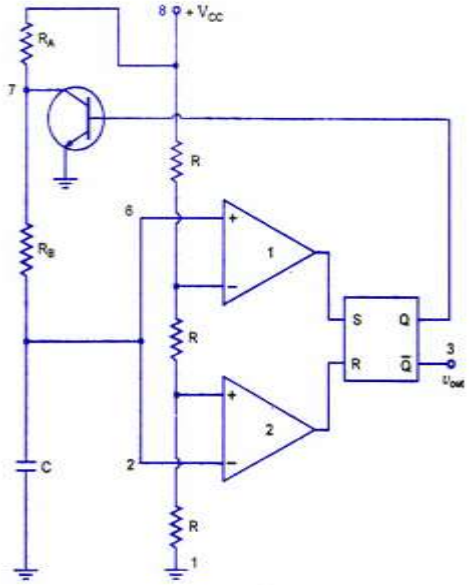
$$f_r = \frac{1}{2\pi RC\sqrt{2N}}$$

If a three-stage RC phase-shift network is connected between this input and output of the amplifier, the total phase shift necessary for regenerative feedback will become 3 x 60^o + 180^o = 360^o

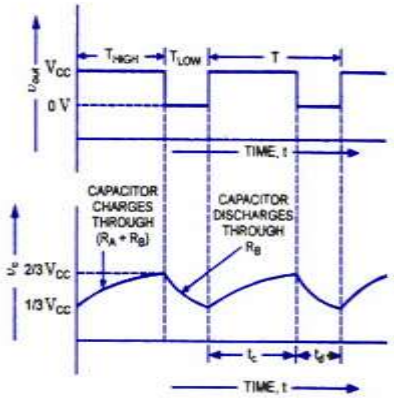
(b) when Q is low or output V_{OUT} is high, the discharging transistor is cut-off and the capacitor C begins charging toward V_{CC} through resistances R_A and R_B. Because of this, the charging time constant is (R_A + R_B) C. Eventually, the threshold voltage exceeds +2/3 V_{CC}, the comparator 1 has a high output and triggers the flip-flop so that its Q is high and the timer output is low. With Q high, the discharge transistor saturates and pin 7 grounds so that the capacitor C discharges through resistance R_B with a discharging time constant R_B C. With the discharging of capacitor, trigger voltage at inverting input of comparator 2 decreases. When it drops below 1/3V_{CC}, the output of comparator 2 goes high and this reset the flip-flop so that Q is low and the timer output is high. This proves the auto-transition in output from lo[illegible]us the cycle repeats.



Circuit of The Timer 555 as an Astable Multivibrator

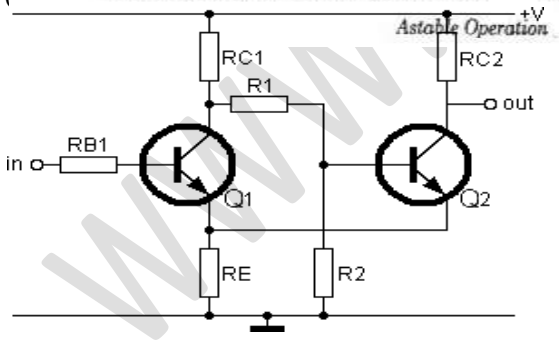


Internal Circuitry With External Connections



Capacitor and Output Voltage Waveforms

X (



Astable Operation

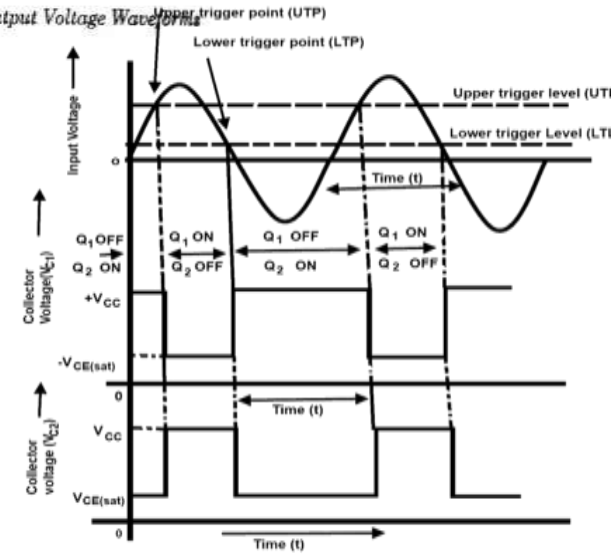


Figure 2: Waveforms at the input and collector of transistor Q1 and Q2

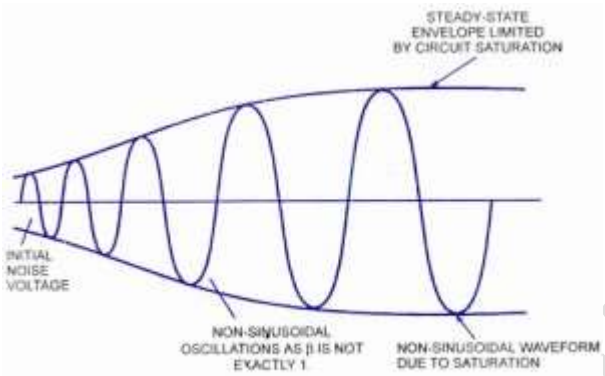
A.C. signal is applied at the input of the Schmitt trigger (i.e. at the base of the transistor Q_1). As the input voltage increases above zero, nothing will happen till it crosses the upper trigger level (U.L.T). As the input voltage increases, above the upper trigger level, the transistor Q_1 conducts. The point, at which it starts conducting, is known as upper trigger point (U.T.P). As the transistor

Q_1 conducts, its collector voltage falls below V_{CC}. This fall is coupled through resistor R_1 to the base of transistor Q_2 which reduces its forward bias. This in turn reduces the current of transistor Q_2 and hence the voltage drop across the resistor R_E. As a result of this, the reverse bias of transistor Q_1 is reduced and it conducts more. As the transistor Q_1 conducts more heavily, its collector further reduces due to which the transistor Q_1 conducts near cut-off. This process continues till the transistor Q_1 is driven into saturation and Q_2 into cut-off. At this instant, the collector voltage levels are $V_{C1} = V_{CE(sat)}$ and $V_{C2} = V_{CC}$ as shown in the figure.The transistor Q_1 will continue to conduct till the input voltage falls below the lower trigger level (L.T.L). It will be interesting to know that when the input voltage becomes equal to the lower trigger level, the emitter base junction of transistor Q_1 becomes reverse biased. As a result of this, its collector voltage starts rising toward V_{CC}. This rising voltage increases the forward bias across transistor Q_2 due to which it conducts. The point, at which transistor Q_2 starts conducting, is called lower trigger point (L.T.P). Soon the transistor Q_2 is driven into saturation and Q_1 to cur-off. This completes one cycle. The collector voltage levels at this instant are $V_{C1} = V_{CC}$ and $V_{C2} = V_{CE(sat)}$. No change in state will occur during the negative half cycle of the input voltage.

(b) Certain conditions are required to be fulfilled for sustained oscillations and these conditions are that

(i) The loop gain of the circuit must be equal to (or greater than) unity and

(ii) The phase shift around the circuit must be zero. These two conditions for sustained oscillations are called Barkhausen ***criteria***.



Buildup of Steady-state Oscillations