TED (10)-3068 Reg. No.....

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THIRD SEMESTER DIPLOMA EXAMINATION IN ENGINEERING/ TECHNOLOGY-MARCH, 2013

COMPUTER ARCHITECTURE

(Common for CM, CT and IF)

[*Time:* 3 hours

(Maximum marks: 100)

Marks

PART –A

(Maximum Mark:10)

I Answer the following questions in one or two sentences. Each question carries 2 marks

1. Write the function of instruction register and instruction pointer

Instruction Register:- holds the instruct**ion** that is currently being executed

Instruction Pointer: It holds the address of the next instructions to be fetched

2. write syntax of two assembler directives.

Label Operation Operand(s) Comment

Syntax: SUM EQU 200

SUM ORIGIN 204

3. Expand PCI and SCSI.

PCI:-Peripheral Component Interconnect

SCSI:- Small Computer System Interface.

4. State the method of differential signalling in rambus memory

The reference voltage is about 2V , and the two logic values are represented by 0.3V swings above and below V_{ref} , such signalling method is used is known as differential signalling

5. Define Microinstructions

- **Micro instruction:** the individual control words in this micro routine is called micro instruction.

PART-B

II Answer *any five* of the following. Each question carries 6 marks.

1.Explain the classification of computers based on speed, size and memory capacity

Many types of computers exist that differ widely in size, cost, computational power, and intended use.

- Personal Computer:- used in homes, schools, and business offices, it has processing and storage units, visual display and audio output units, and a keyboard that can all be located easily on a home or office.
- Notebook computers:- It has high resolution Graphics input/output capability.
- Workstations:- used in engineering applications, especially for interactive design work.
- Enterprise systems(mainframes):- used for business data processing in medium to large corporations that require much more computing power and storage capacity than workstations.
- Super Computers:- used for large-scale numerical calculations required in applications such as weather forecasting and aircraft design and simulation.

2. Write notes on: (a) Super Scalar architecture:

Execution of several instructions is possible in a given time slot, this activity is referred as super scalar operation.

(b) pipelining:

The processor need not wait till the execution of instruction one in order to execute instruction two, rather the processor directly starts executing instruction two, while the instruction one is under execution, this is referred to as pipelining.

3. differentiate between memory mapped I/O and I/O mapped I/O

Memory mapped I/O.

-I/O devices and the memory may share the same address space

-any machine instruction that can access memory can be used to transfer data to or from an I/O device

I/O mapped I/O

-I/O devices and the memory may have different address space

-special instructions to transfer data to and from I/O devices

-I/O devices may have to deal with fewer address lines

4. Describe the sequence of events of data transfer in SCSI

1. The SCSI controller ,acting as an initiator,contents for control of the bus.
2. When the initiator wins the arbitration process,it selects the target controller and hands over control of the bus to it
3. The target starts an output operation (from initiator to target)., in response to this,the initiator sends a command specifying the required read operation
4. The target, realizing that it first needs to perform a disk seek operation , sends a message to the initiator indicating that it will temporarily suspend the connection between them. Then it releases the bus
5. The target controller sends a command to the disk drive to move the read head to the first sector involved in the requested read operation.then, it reads the data stored in the sector an stores them in a data buffer.
6. The target transfers the contents of data buffer to the initiator and then suspends the connection again. data are transferred either 8 or 16 bits in parallel depending on the width of the bus.
7. The target controller sends a command to the disk drive to perform another seek operation.then,it transfers the contents of the second disk sector to the initiator,as before.at the end of this transfer,the logical connection between the two controllers is terminated
8. As the initiator controller receives the data,it stores them into the main memory using the DMA approach.
9. The SCSI controller sends an interrupt to the processor to inform it that the requested operation has been completed.

5. Write notes on : (a) EPROM:

-EPROM(Erasable Programmable Read Only Memory):

-It is an erasable PROM.
-Its contents can be erased and can be reprogrammed more than once.
-It stores a bit by charging the floating gate of an FET.
-Information is stored by using an EPROM programmer,which applies high voltage to charge the gate

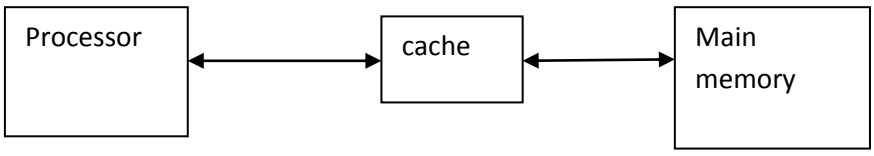
(b) Flash Memory:

-it is electrically erasable and programmable.

-the memory chip can be erased and reprogrammed at least a million times.

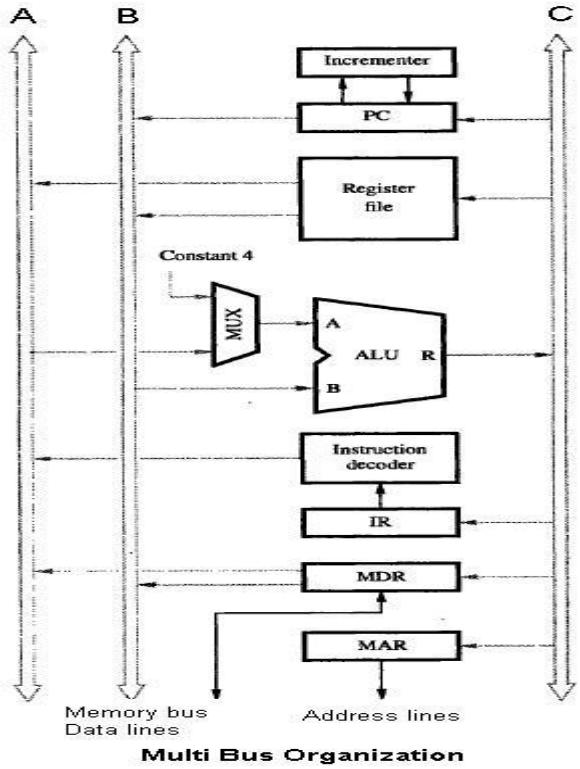
6. Explain the working of cache memory

- The CPU of a computer can usually process instructions and data faster than they can be fetched from a reasonably priced main memory unit.
- Using a cache memory, the memory cycle time can be reduced.
- A cache is small, fast memory that is inserted between the larger, slower main memory and the CPU as in.



- Cache is a semiconductor memory. It consists of SRAM's. Its access time is about ions which is less than that of the main memory (50 ns).
- The modern 32-bit and 64-bit microprocessors operate at very high speed.
- There are two types of cache schemes---write through and write back.
- Here both the main memory and cache contains the same data which is a desirable characteristic for direct memory access (DMA).
- This required additional hardwired support, but improves performance, since the exchanges between cache and the main memory are fewer and better timed.
- Cache is placed at two or three levels, called first level(L_1), second level(L_2), third level(L_3).

7. Draw the architecture of three-bus organization.



Multi Bus Organization

PART—C

(Answer one full question from each unit. Each question carries 15 marks.)

UNIT--I

III Explain the different factors that affect the performance of a computer system. 15

Performance is measured in terms of its accessing capability. Hence, performance is nothing but, how fast a computer executes programs. the accessing speed of a computer basically depends on three entities, they are

1. The hardware circuitry through which the computerise made.

2. the design of various instruction sets, supported by a computer.

3.the design of different compilers,which are used in compiling a set of programs.

Processor clock:

In order to organize or schedule the processors activities, a clock is embedded on its circuit board which is referred as processor clock.hence, a given processor performs its activities depending on its clock cycles.

Basic performance equqtion:

$$T=\frac{N\times S}{R}$$

Where,

T-processor time required to execute a program that has been prepared in high-level language

N-number of actual machine language instructions needed to complete the execution (note:loop)

S-average number of basic stepe needed to execute one machine instruction.Each step completes in one clock cycle

R-clock rate

Pipelining and superscalar operation:

The processor need not wait till the execution of instruction one in order to execute instruction two, rather the processor directly starts executing instruction two, while the instruction one is under execution, this is referred to as pipelining.

Execution of several instructions is possible in a given time slot, this activity is referred as super scalar operation.

Clock rate:

In basic performance equation

$$T=\frac{N\times S}{R}$$

The quantity 'R' is referred as clock rate which is measured in terms of cycles per second.

CISC and RISC:

Complex Instruction set Computer (CISC) refers to a type of processors which possesses ability to implement certain complex instructions

Reduced Instruction set computer (RISC) refers to another variety of processors which implements a concept such as every instruction is valid to acquire only single word.

Compiler:

A compiler is a program which translates a given high level language program into machine level by passing it through sequence of predefined steps.

Performance measurement:

To measure the performance of the system a new organization was found under the name SPEC or system performance evaluation corporation. This organization framed certain demonstrating program and executed them on different systems.

OR

IV Write short notes on: **(3× 5 = 15)**

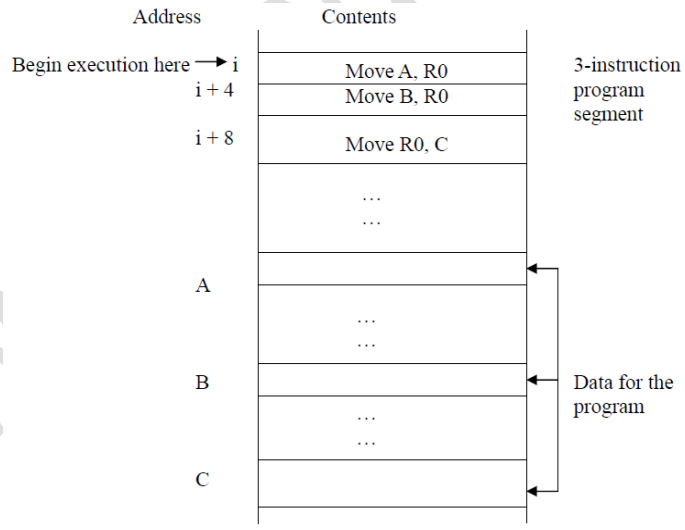
(a) Assembly process.

Machine Instructions are represented by patterns of 0s and 1s. We use symbolic names to represent the patterns.So far we have used normal words,such as Move, Add , Increment and branch.

-when writing programs for a specific computer, such words are normally replaced by acronyms called mnemonics, such as MOV,ADD,INC and BR.

-A complete set of rules for using the mnemonics in the specification of complete instruction and programs is called the syntax of the language.

(b) Straight line sequencing



one memory operand per instruction
-32-bit word length
-Memory is byte addressable
-full memory address can be directly specify in a single word instruction

To begin executing a program, the address of its first instruction must be placed into the PC.Then the processor control circuit use the information in the PC to fetch and execute

instructions,one at a time,in order of increasing addresses,This is called straight line sequencing

During the execution of each instruction the PC incremented by 4 to point to the next instruction

(c) Conditional codes

Conditional code flags/conditional code register/status register

- N(negative):set to 1-if the result is negative;otherwise cleared to 0
- Z(zero):set to 1-if the result is zero;otherwise,cleared to 0
- V(overflow): set to 1-if arithmetic overflow occurs;otherwise cleared to 0
- C(carry): set to 1-if a carry out results from the operation;otherwise,cleared to 0
- Different instructions affect different flags

UNIT—II

V (a) Describe the working of interrupt driven I/O. **5**

The problem with programmed I/O is that the processor has to wait a long time for the I/O module of concern to be ready for either reception or transmission of data.
The processor, while waiting, must repeatedly interrogate the status of the I/O module.

This type of I/O operation, where the CPU constantly tests a part to see if data is available, is polling, that is, the CPU Polls (asks) the port if it has data available or if it is capable of accepting data. Polled I/O is inherently inefficient.

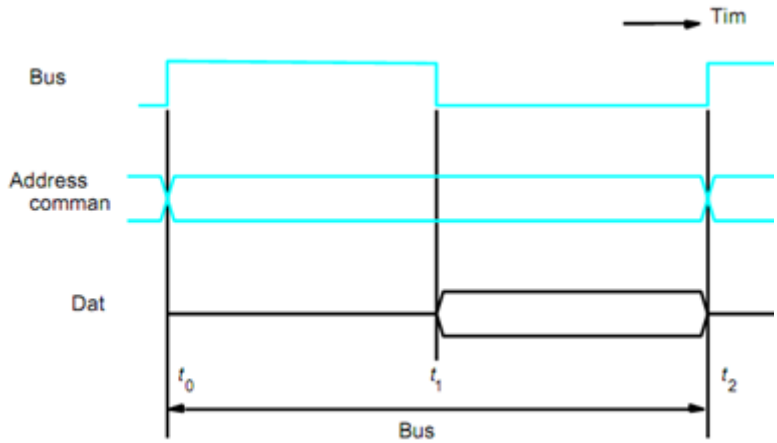
The solution to this problem is to provide an interrupt mechanism. In this approach the processor issues an I/O command to a module and then go on to do some other useful work. The I/O module with then interrupt the processor to request service when it is ready to exchange data with the processor. The processor then executes resumes its former processing.

V(b) write notes on (a) Synchronous bus: **($2\times 5 = 10$)**

-All devices derive timing information from a common clock signal

-At time $t_{0,}$ the processor places the device address on the address lines of system bus and sets the control lines to perform the input operation.

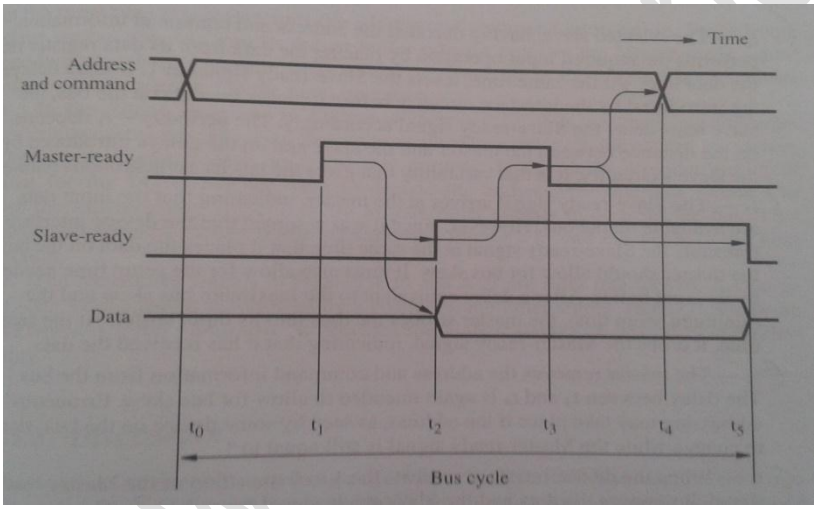
-the clock pulse width should be chosen such that it is greater than the maximum propagation delay between the processor and any of the devices connected to the bus.



(b) Asynchronous bus

In asynchronous bus, the common clock is eliminated and data transfer on the system bus is achieved by the use of a handshake between the processor and the device being addressed. here.

the clock line is replaced by two control signals ready and accept



OR

VI (a) Explain the method of recognizing and handling multiple interrupt requests. 10

-A request is received over the common interrupt request line.additional information is needed to identify the particular device that activated the line.

-It two devices have activated the line at the same time,it must be possible to break the tie and select one of the two requests for service.when an interrupt service routine for the selected device has been completed,the second request can be serviced

The information needed to determine whether a device is requesting an interrupt is available in its status register.when a device raises an interrupt request, it sets to 1 one of the bits in its status register,which will call the IRQ bit

-the simplest way to identify the interrupting device is to have the interrupt service routine poll all the I/O devices connected to the bus.the first device encountered with its IRQ bit set is the device that should be serviced.An appropriate subroutine is called to provide the requested service.

-the polling scheme is easy to implement.its main disadvantage is the time spent interrogating the IRQ bits of all the devices may not be requesting any service.

Vectored Interrupts:

To reduce the time involved in the polling process,a device requesting an interrupt may identify itself directly to the processor.then, the processor can immediately start executing the corresponding interrupt-service routine.

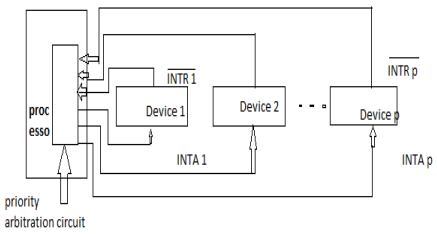
-the term vectored interrupts refers to all interrupt-handling schemes based on this approach.

-a device requesting an interrupt can identify itself by sending a special code to the processor over the bus.this enables the processor to identify individual devices even if they share a single interrupt-request line.

Interrupt nesting:

-Execution of a given interrupt-service routine,once started ,always continues to completion before the processor accepts an interrupt request from a second device.

-interrupt –service routine are typically short,and the delay they may cause in acceptable for most simple devices.



Simultaneous requests:

-the processor must have some means of deciding which request to service first. The processor simply accepts the request having the highest priority.if several devices share once interrupt –request line.

Controlling device requests:

-it is important to ensure that interrupt requests are generated only by those I/O devices that are being used by a given program.Idle devices must not be allowed to generate interrupt requests,even though they may be ready to participate in I/O transfer operations.

VI(b) Explain the working of direct memory access. 5

DMA consists of a special control unit which is provided to transfer a block of data directly between an I/O device and the main memory without intervention by the processor.

-when the processor determines that the program that is being executed requires a DMA transfer,it informs the DMA controller which sits in the interface circuit of the device of three things,namely,the starting address of the memory location,the number of words that needs to be transferred,and the direction of transfer that is,whether the data needs to be transferred from the I/O device to the memory or from the memory to the I/O device.

-after initiating the DMA transfer,the processor suspends the program that that initiated the transfer,and continues with the execution of some other program.the program whose execution is suspended is said to be in the blocked state.

-usually,the processor originates most cycles on the bus.the DMA controller can be said to steal memory access cycles on from the bus thus,the processor and the DMA controller use the bus in an interwoven fashion.this interweaving technique is called as cycle stealing

UNIT—III

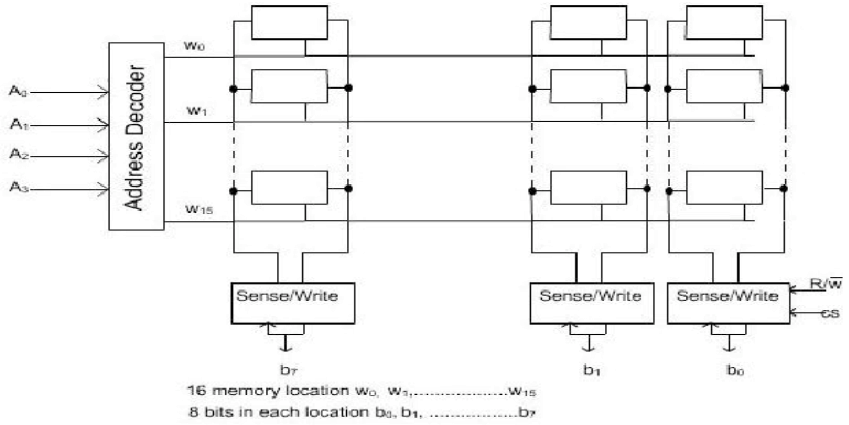
VII With a neat diagram , explain the organization of a bit cell in memory. 15

each memory cell can hold one bit of information.
-memory cells are organized in the form of an array.
-one row is one memory word.
-all cells of a row are connected to a common line,known as the “word line”.
-word line is connected to the address decoder.

-sense/write circuits are connected to the data input/output lines of the memory chip.

Commercially available memory chips contain a much larger number of memory cells than the above.

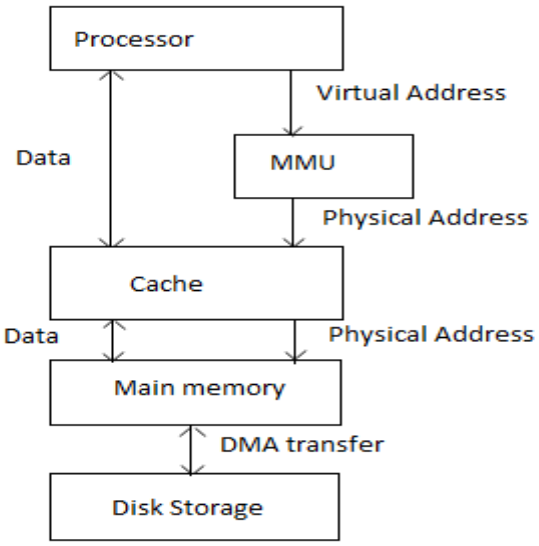
- Large chips have essentially the same organization , but use a larger memory cell array and have more external connections.
- - For example: a 4M-bit chip may have a 512K x 8 organization. In which case 19 address and 8 data input/output pins are needed.now available
- - chips with a capacity of hundreds of megabits



OR

VIII (a) Explain the organization of virtual memory with neat sketch. 8

- Virtual memory is an architectural solution to increase the effective size of the memory system
- Physical main memory in a computer is generally not as large is the entire possible addressable space.
  - ♦ Physical memory typically ranges from a few hundred megabytes to 1 G bytes.
- Techniques that automatically move program and data between main memory and secondary storage when they are required for execution are called virtual memory techniques.
- Programs and processors reference an instruction or data independent of the size of the main memory
- Processor issues binary addresses for instructions and data.
  - These binary addresses are called logical or virtual addresses
- Virtual addresses are translated into physical addresses by a combination of hardware and software subsystems.
  - ♦ If virtual addresses refers to a part of the program that is currently in the main memory,it is accessed immediately.
  - ♦ If the address refers to a part of the program that is not currently in the main memory,it is first transferred to the main memory before it can be used.



If the desired data or instructions are in the main memory they are fetched

- If the desired data or instructions are not in main memory, they must be transferred from secondary storage to the main memory.
- MMU causes the operating system to bring the data from the secondary storage into the main memory.

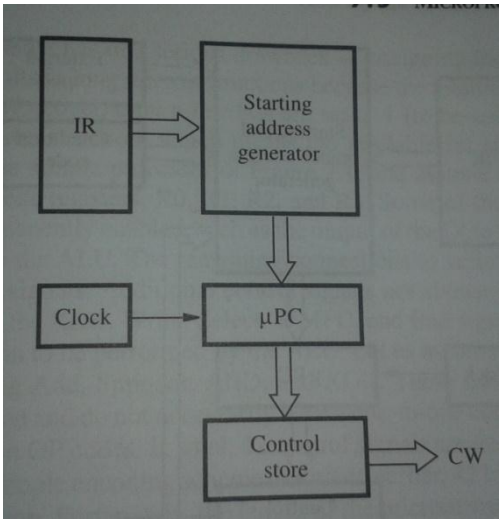
VIII (b) Explain the working of optical disks. 7

- These store the data on a reflective surface so it can be read by a beam of laser light
- A laser uses a concentrated , narrow beam of light, focused and directed with lenses,prisms,and mirrors.
  - CD-ROM
- CD-ROM drive reads digital data from a spinning disks by focusing on the disks's surface.
- Some areas of the disks reflect the laser light into a sensor,and other areas scatter the light.
- A spot that reflected the laser beam into the sensor is interpreted as a 1, otherwise 0.
- Data in the form of ***lands.***
- ***Flat area on the metal surface.***
- Pits : depressions or hollows.

UNIT—IV

IX (**a**)**With neat diagram, explain the organization of micro programmed control units. 10**

- Control signals are generated by a program similar to machine language programs.
- When a new instruction is loaded into the IR , the Micro PC is loaded with the starting address of the micro routine for that instruction.
- **Control word(CW);** Is a word whose individual bits represent the various control signals. Each of the control steps in the control sequence of an instruction defines a unique combination of 1s and 0s in the CW
- **Microroutine:** A sequence of CWs corresponding to the control sequence of a machine instruction constitutes the microroutines.
- **Micro instruction:** the individual control words in this microroutine is called micro instruction.



- A straight forward way to structure microinstructions is to assign one bit position to each control signal
- However,this is very inefficient.
- The length can be reduced; most signals are not needed simultaneously,and many signals are mutually exclusive.
- All mutually exclusive signals are placed in the same group in binary coding

IX b . Explain the role of cache in pipelining **5**

- **E**ach pipeline stage is expected to complete in one clock cycle.
- The clock period should be long enough to let the slowest pipeline stage to complete
- Faster stage can only wait for the slowest one to complete.
- Since main memory is very slow compared to the execution, if each instruction needs to be fetched from main memory, pipeline is almost useless.
- The use of cache memories solves the memory access problem.

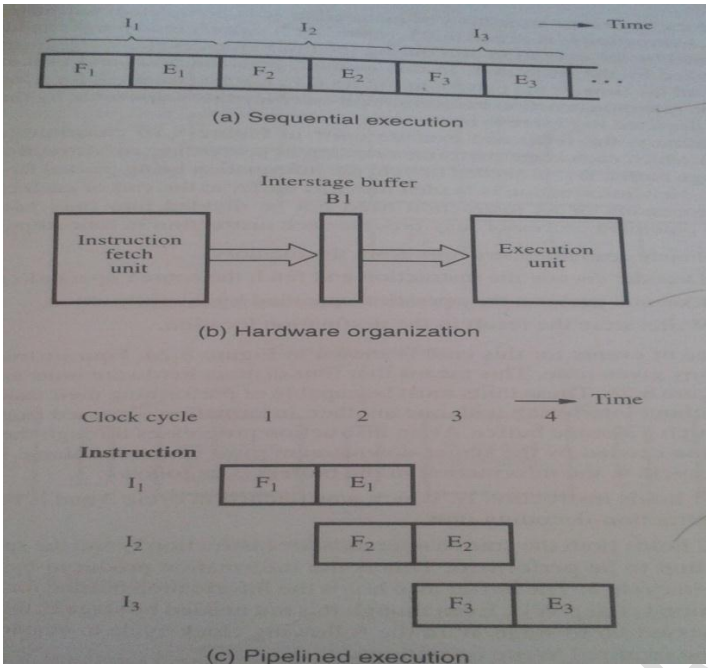
OR

X (a) Describe the basic concepts of pipelining. **10**

Pipelining is a particularly effective way of organizing concurrent activity in a computer system.

The basic idea is very simple.

-the processor executes a program by fetching and executing instructions, one after the other.



-let F1 and E1 refer to the fetch and executes steps for instruction I1

-execution of a program consists of a sequence of fetch and execute steps

- In another step, separate hardware organization for Instruction fetch and Execution step.

Fetched instruction is deposited in to the intermediate interstage buffer B1,then the execution hardware take this instruction from the buffer and execute.

- In pipelined execution, a clock cycle is provided; fetching and execution for one instruction may take place within one clock cycle.

X (b) Explain the process of fetching a word from memory. 5

To fetch a word of information from memory, the processor has to specify the address of the memory location where this information is stored and request a read operation.

This applies whether the information to be fetched represents an instruction in a program or an operand.

Specified by an instruction. The processor transfers the required address to the MAR, whose output is connected to the address lines of the memory bus.

At the same time,the processor uses the control lines of the memory bus to indicate that a read operation is needed.