TED (10)-3068 Reg. No.....

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THIRD SEMESTER DIPLOMA EXAMINATION IN ENGINEERING/ TECHNOLOGY-MARCH,2014

**COMPUTER ARCHITECTURE**

(Common for CM, CT and IF)

[*Time:* 3 hours

(Maximum marks: 100)

Marks

PART –A

(Maximum mark:10)

I Answer the following questions in one or two sentences. Each question carries 2 marks

**1 Role of MAR register**

It holds the address of the location to be accessed

**2. Describe assembler.**

Programs written in an assembly language can be automatically translated into a sequence of machine instructions by a program called an assembler.

**3. Name the registers used in the DMA operation.**

- Starting Address register
- Word count register
- Status register

**4.Write the role of Cache memory.**

- **E**ach pipeline stage is expected to complete in one clock cycle.
- The clock period should be long enough to let the slowest pipeline stage to complete
- Faster stage can only wait for the slowest one to complete.
- Since main memory is very slow compared to the execution, if each instruction needs to be fetched from main memory, pipeline is almost useless.
- The use of cache memories solves the memory access problem.

**5.Functions of Micro Program counter.**

- Used to count the control signals produced
- It is used to read control words sequentially from the control store

## PART-B

**II Answer *any five* of the following. Each question carries six marks.**

1. **Describe pipelining and super scalar operations.**
   The processor need not wait till the execution of instruction one in order to execute instruction two, rather the processor directly starts executing instruction two, while the instruction one is under execution, this is referred to as pipelining.
   Execution of several instructions is possible in a given time slot, this activity is referred as super scalar operation.

2. **Explain the different types of computer.**

   **Personal Computer:** which has found wide use in homes, Schools,and business offices. It is the most common form of desktop computers.

   **Notebook Computers:** Compact version of the personal computer with all of these components packaged into a single unit the size of a thin briefcase.

   **Workstations:** high resolution graphics input/output capability, although still retaining the dimensions of desktop computers.

   **Enterprise systems:** a range of large and very powerful computer systems exists

   **Supercomputers:** it works at high end.

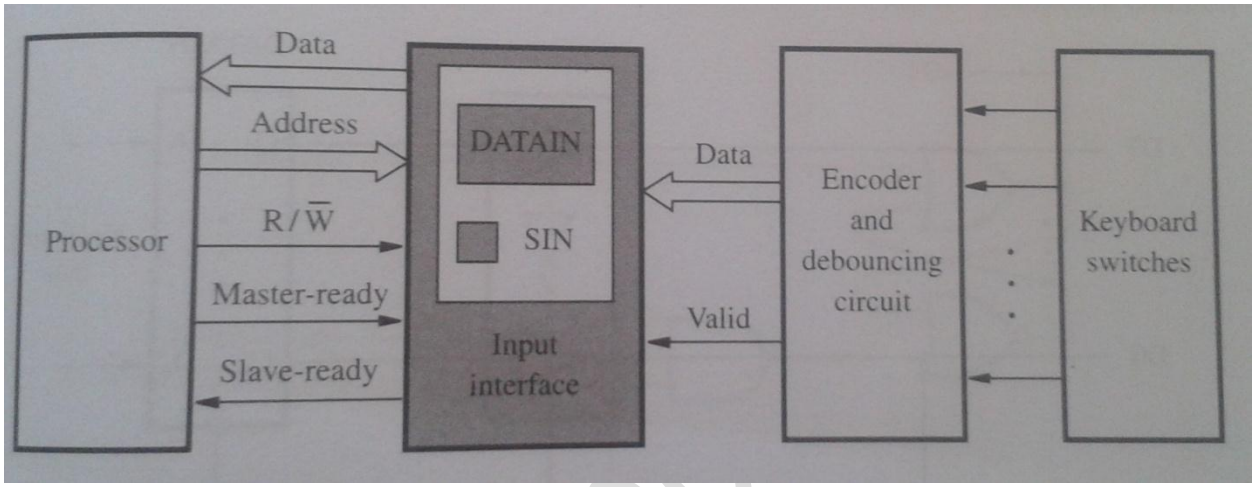
   **Mainframes:** used for business data processing in medium to large corporations that require much more computing power and storage capacity than workstations can provide

3. **Discuss the steps of interrupt handling.**

   -processor is executing the instruction located at address i when an interrupt occurs- routine executed in response to an interrupt request is called the interrupt service routine
   -when an interrupt occurs, control must be transferred to the interrupt service routine
   -but before transferring control,the current

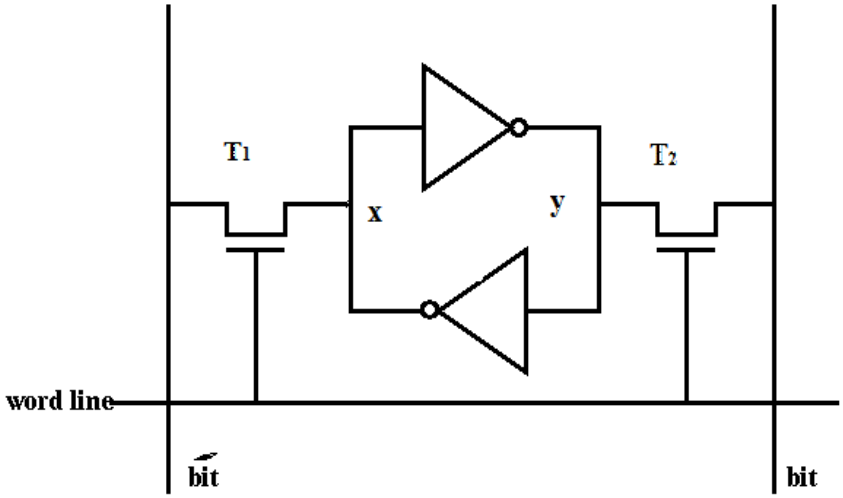
Contents of the PC(i+1),must be saved in a known location.
-this will enable the return –from-interrupt to resume execution at i+1.
-return address, or the contents of the PC are usually stored on the processor stack.

4. **Draw the parallel port interface connection from keyboard to processor.**




5. **Draw the SRAM cell and explain it parts.**

Two transistors
Two invertors
Bit lines




6. **Discuss the temporal locality of reference and spatial locality of reference.**

-Temporal locality: it suggests that whenever an information item(instruction or data) is first needed, this item should be brought into the cache when it will hopefully remain until it is needed again.

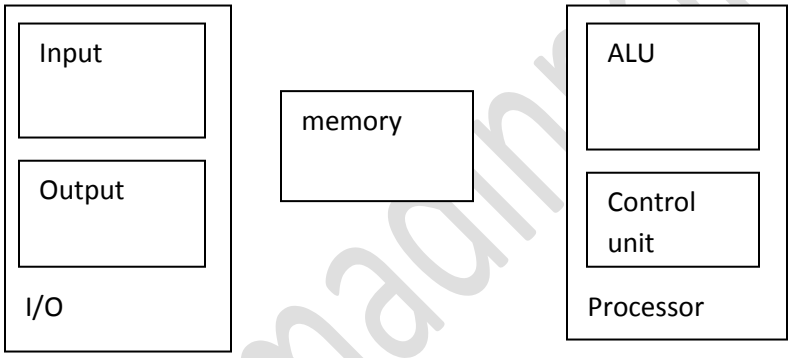
-Spatial Locality: instead of fetching just one item from the main memory to the cache , it is useful to fetch several items that reside at adjacent addresses as well.

7. **What is sequence of operations to add the contents of register R1 to those of R2 and store the result in R3?**
    1. **$R_{1\ out}$, $Y_{in}$**
    2. **$R_{2\ out}$, Select Y , Add, $Z_{in}$**
    3. **$Z_{out}$, $R_{3\ in}$**

**PART—C**

(Answer one full question from each unit. Each question carries 15 marks.)

**III Explain the functional units of a computer.** **15**




A computer consists of five functionally independent main parts: input, memory, arithmetic and logic, output, and control units

- The input unit accepts the coded information from human operators, from electromechanical devices such as keyboards, or from other computers over digital communication lines.
- This information received is either stored in the computer's memory for later references or immediately used by the arithmetic and logic circuitry to perform the desired operation.
- The results are sent back to the outside world through the output unit
- **Input Unit:**
    - Computers accept coded information through input units, which read the data.
    - EX: Keyboard
        - Whenever a key is pressed,the corresponding letter or digit is automatically translated into its corresponding binary code and transmitted over a cable to either the memory or the processor.
- **Memory Unit:**
    - The function of the memory unit is to store programs and data.
    - There are two classes of storage, called primary and secondary.

- Programs must reside in the memory during execution.Instruction and data can be written into the memory or read out under the control of the processor

- **Arithmetic and Logic:**
  - Most computer operations are executed in the arithmetic and logic unit(ALU) of the processor.
  - EX: consider two numbers located in the memory are added.they are brought in to the processor,and the actual addition is carried out by the ALU.The sum may then be stored in the memory or retained in the processor for immediate use.
- **Output Unit:**
  - Its function is to send Processed results to the outside world
  - EX: Printer, Monitor etc
- **Control Unit:**
  - The control unit is effectively the nerve center that sends control signals to the other units and senses their states.

**OR**

**IV Discuss the performance of a computer system with the support of basic performance equation.** **15**

Performance is measured in terms of its accessing capability. hence, performance is nothing but,how fast a computer executes programs.the accessing speed of a computer basically depends on three entities,they are

1.The hardware circuitry through which the computeris made.

2.the design of various instruction sets,supported by a computer.

3.the design of different compilers,which are used in compiling a set of programs.

**Processor clock:**

In order to organize or schedule the processors activities, a clock is embedded on its circuit board which is referred as processor clock.hence, a given processor performs its activities depending on its clock cycles.

**Basic performance equqtion:**

$$T=\frac{N\times S}{R}$$

Where,

T-processor time required to execute a program that has been prepared in high-level language

N-number of actual machine language instructions needed to complete the execution (note:loop)

S-average number of basic stepe needed to execute one machine instruction.Each step completes in one clock cycle

R-clock rate

**Pipelining and superscalar operation:**

The processor need not wait till the execution of instruction one in order to execute instruction two, rather the processor directly starts executing instruction two, while the instruction one is under execution, this is referred to as pipelining.

Execution of several instructions is possible in a given time slot, this activity is referred as super scalar operation.

**Clock rate:**

In basic performance equation

$T=\frac{N\times S}{R}$

The quantity 'R' is referred as clock rate which is measured in terms of cycles per second.

**CISC and RISC:**

Complex Instruction set Computer (CISC) refers to a type of processors which possesses ability to implement certain complex instructions

Reduced Instruction set computer (RISC) refers to another variety of processors which implements a concept such as every instruction is valid to acquire only single word.

**Compiler:**

A compiler is a program which translates a given high level language program into machine level by passing it through sequence of predefined steps.

**Performance measurement:**

To measure the performance of the system a new organization was found under the name SPEC or system performance evaluation corporation. this organization framed certain demonstrating program and executed them on different systems.

**Unit II**

**V (a) Discuss the serial port communication with a diagram. 10**

A serial port is a communication physical interface through which information transfers in or out one bit at a time.

-it is capable of communicating in a bit serial fashion on the device side and in a bit parallel fashion on the bus side.

-the transformation between the parallel and the serial formats is achieved with shift registers that have parallel access capability.

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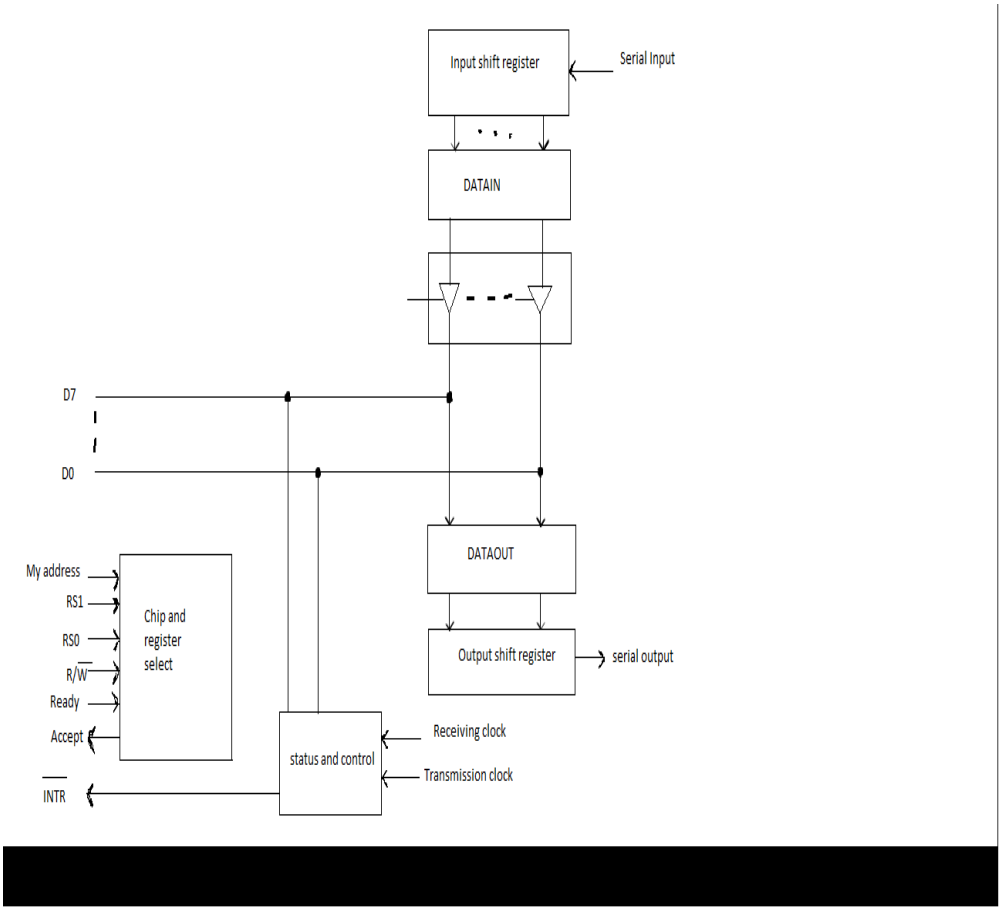



-the part of the interface that deals with the bus is the same as in the parallel interface.

-the double buffering used in the input and output paths is important. a simpler interface could be implemented by turning DATAIN and DATAOUT into shift registers and eliminating the shift registers –

-because serial interfaces play a vital role in connecting I/O devices, several widely used standards have been developed.

**V (b) Merits of serial communication** **5**

Used in applications such as industrial automation systems and some industrial and consumer products.

Server portas a control console for diagnostics.

Serial ports are still used in these areas as they are simple, cheap and functions are highly standardized and widespread.

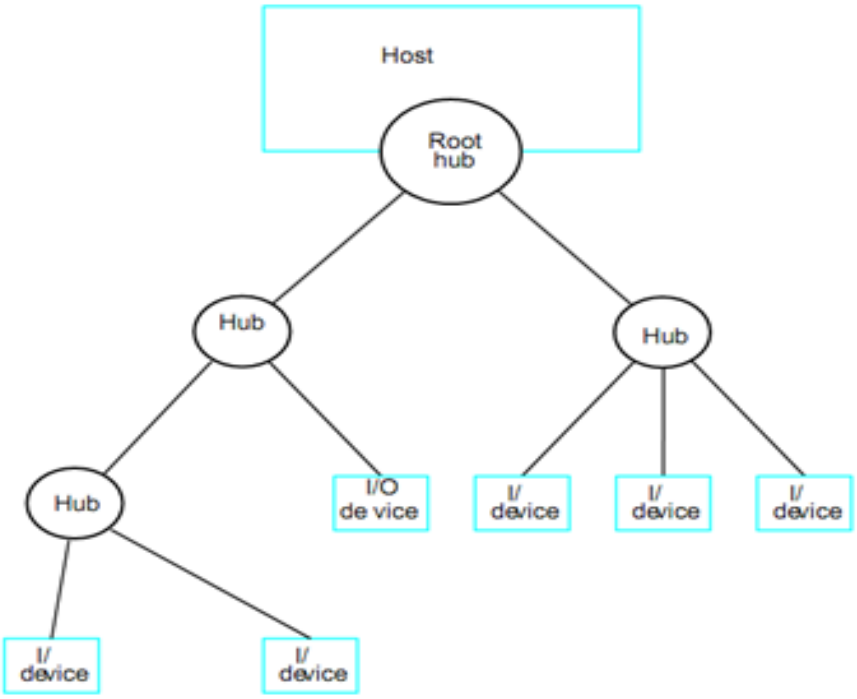
**OR**

**VI (a) Draw and Explain the USB Structure.** **10**

- speed
- Low-speed(1.5 Mb/s)
- Full-speed(12 Mb/s)

High-speed(480 Mb/s)

- To accommodate a large number of devices that can be added or remove data any time, the USB has the tree structure as shown in the figure
- -Each node of the tree has a device called a hub, which act as an intermediate control point between the host and the I/O devices.
- -at the root of the tree, a root hub connects the entire tree to the host computer. the leaves of the tree are the I/O devices being served(for example, keyboard, internet connection, speaker or digital TV).
- -in normal operation, a hub copies a message that it receives from its upstream connection to all its downstream ports. As a result, a message sent by the host computer is broadcast to all I/O devices, but only the addressed device will respond to that message.
- However , a message from an I/O device is sent only upstream towards the root of the tree and is not seen by other devices. Hence, the USB enables the host to communicate with the I/O devices, but it does not enable these devices to communicate with each other.

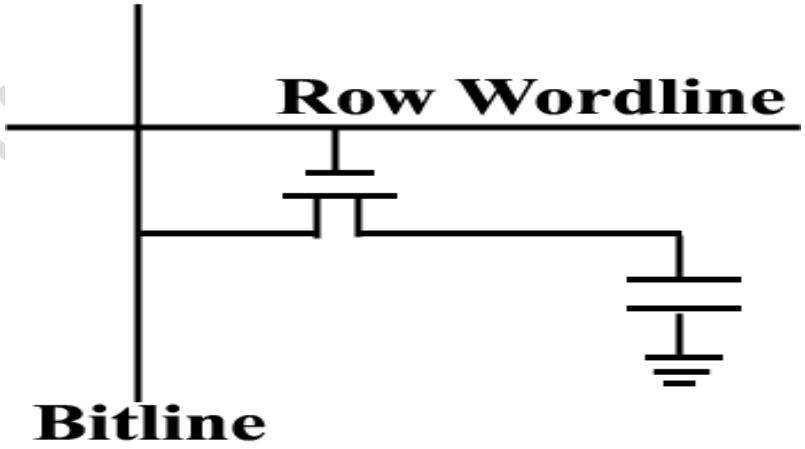



**VI (b) Explain the polling scheme in interrupt** **5**

- If the processor uses a polling mechanism to poll the status registers of I/O devices to determine which device is requesting an interrupt. In this case the priority is determined by the order in which the devices are polled. The first device with status bit set to 1is the device whose interrupt request is accepted

**UNIT III**

**VII (a) Explain single transistor DRAM cell** **10**



- Memory cells do not retain their state indefinitely.
- Information stored in a dynamic memory cell in the form of a charge on a capacitor, and this charge can be maintained for a much longer time, its contents must be periodically refreshed by restoring the capacitor charge to its full value.
- The timing of the memory device is controlled asynchronously. A specialized memory controller circuit provides the necessary control signals, RAS and CAS, that govern the timing.the processor must take into account the delay in the response of the memory.
- Such memories are referred to as asynchronous DRAMs.
- Because of their high density and low cost, DRAMs are widely used in the memory units of computers.

**VII (b) Describe Memory latency and Memory Bandwidth. 5**

Memory latency is the time its takes to transfer a word of data to or from memory

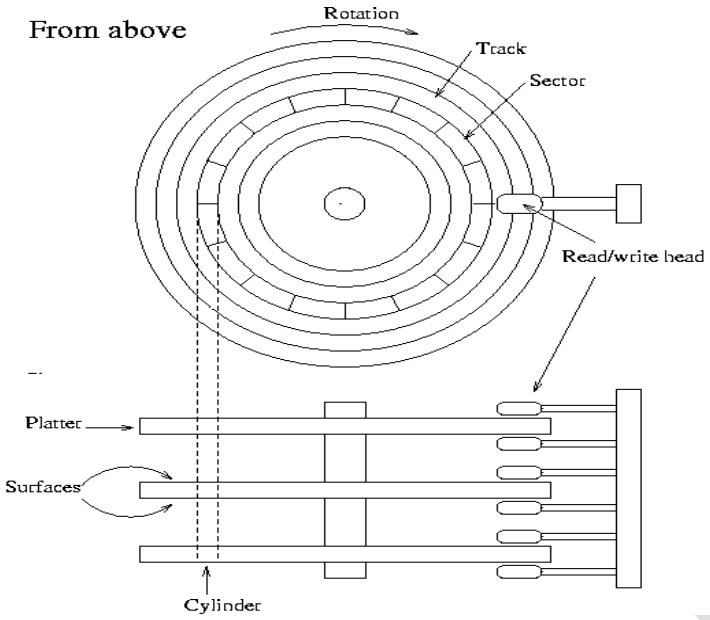
In the case of reading or writing a single word of data, the latency provides a complete indication of memory performance.

Memory bandwidth is the number of bits or bytes that can be transferred in .The effective bandwidth in a computer system is not determined by solely by the speed of the memory

**OR**

**VIII Explain the magnetic hard disk and its working 15**

- A magnetic hard disk is circular plate constructed of metal or plastic coated with magnetized material. Often both sides of the disk are used and several disks may be stacked on one spindle with read/write heads available on each surface.
- All disks rotate together at high speed and are not stopped or started for access purposes.
- Bits are stored in the magnetized surface in spots along concentric circles called tracks. the tracks are divided into sectors.
- The minimum quantity of information which can be transferred is a sector or group of sectors called clusters.

- 


- Here read/write head has to be moved to different tracks for reading and writing. Other units are seperate read/write heads are provided for each track in each surface.
- After the read/write heads are positioned in the specified track .Information transfer is very fast once the beginning of a sector has been reached.
- A track in a given sector near the circumference is longer than a track near the center of the disk.
- To make all the records in a sector of equal length, some disks use a variable recording density with higher density on tracks near the center than on tracks near the circumference.
- Disks are permanently attached to the unit assembly and cannot be removed by the occasional user are called *hard disks*
- A disk drive with removable disk is called a *floppy disk.*
- There are two sizes commonly used magnetic recording materials are:
- (i) 5.25" diameter, 1.2 MB capacity/360 KB capacity
- (ii) 3.5" diameter, 1.44 MB capacity.
- A magnetic hard disk is circular plate constructed of metal or plastic coated with magnetized material. Often both sides of the disk are used and several disks may be stacked on one spindle with read/write heads available on each surface.

**UNIT IV**

**IX Explain the complete steps involved in execution of instruction Add (R3), R1 with the control sequences. 15**

Consider the instruction,

Add (R3) , (R1)

Which adds the contents of memory location pointed to by R1.Executing this instruction requires the following actions:

1. Fetch the instruction.
2. Fetch the first operand (the contents of the memory location pointed to by R1).
3. Perform the addition.
4. Load the result into R3.

The sequence of control steps required to perform these operations for the single bus architecture is given below.

1. $PC_{out}$ ,$MAR_{in}$ , Read , Select4 , Add , $Z_{in}$
2. $Z_{out}$ , $PC_{in}$ , $Y_{in}$ , WMFC
3. $MDR_{out}$ , $IR_{in}$
4. $R1_{out}$ , $MAR_{in}$ , Read
5. $R3_{out}$ , $Y_{in}$ , WMFC
6. $MDR_{out}$ , SelectY , Add, $Z_{in}$
7. $Z_{out}$ , $R1_{in}$ , End

In step 1:- the instruction fetch operation is initiated by loading the contents of the PC into the MAR and sending a read request to the memory. The select signal is set to Select4,which causes the multiplexer MUX to select the constant4. This value is added to the operand at input B and result is stored in the register Z.

Step 2:-The updated value is moved from register Z back into the PC

Step 3:-The word fetched from the memory is loaded into the IR.

Step 4:-The instruction decoding circuits interprets the contents of the IR and the contents of register R3 are transferred to the MAR and a memory read operation is initiated.

Step 5:- The contents of R1 are transferred to register Y

Step 6:- When a read operation is completed, the memory operand is available in register MDR, and the addition operation is performed.

Step 7:-the Sum is stored in register Z.

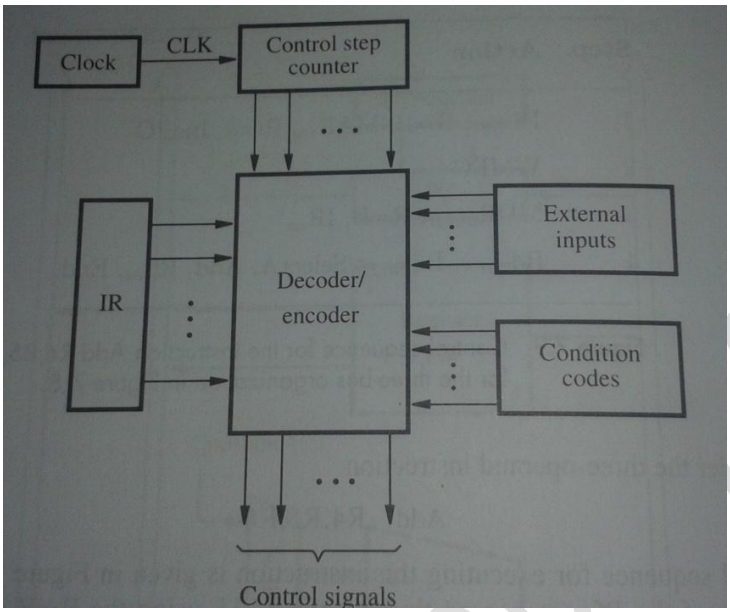
**OR**

**X (a) Explain the hardwired Organization Control unit. 10**

The hardwired control state machine operates at a faster clock rate.

-the control logic is implemented with gates, flip-flops, decoders and other digital circuits.

--it can be optimized to produce a fast mode of operation by having changes in the wiring among the various components.




-**Advantages of hardwired control unit**:

-the hardwired control unit works fast.

-the combinational circuits generate the control signals based on the input signals status.

-the delay between the output generation to input availability depends on the number of gates in the path and propagation delay of each gate in the path.

**-Disadvantages:**

-if the cpu has a large number of control points, the control unit design becomes very complex

-the design does not give any flexibility. if any modification is required, it is extremely difficult to make the correction.

**X (a) Discuss the role of cache memory in pipelining.** **5**

- **E**ach pipeline stage is expected to complete in one clock cycle.
- The clock period should be long enough to let the slowest pipeline stage to complete
- Faster stage can only wait for the slowest one to complete.
- Since main memory is very slow compared to the execution, if each instruction needs to be fetched from main memory, pipeline is almost useless.
- The use of cache memories solves the memory access problem.