TED (10)-3068 Reg. No.....

(REVISION-2010) Signature.....

THIRD SEMESTER DIPLOMA EXAMINATION IN ENGINEERING/ TECHNOLOGY-OCTOBER, 2012

COMPUTER ARCHITECTURE

(Common for CM, CT and IF)

[*Time:* 3 hours

(Maximum marks: 100)

Marks

PART –A

I Answer the following questions in one or two sentences. Each question carries 2 marks

1.List the four basic types of operations that need to be supported by an instruction set

- Data transfer between the memory and the processor registers.
- Arithmetic and logic operations on data
- Program sequencing and control
- I/O transfers

2.State the use of program counter register.

Address of the next instruction to be executed

3. Write the function of interrupt vector

- To reduce the time involved in the polling process by identify the device itself to the processor.

4. **Distinguish between temporal locality and spatial locality**.

-Temporal locality: it suggests that whenever an information item(instruction or data) is first needed, this item should be brought into the cache when it will hopefully remain until it is needed again.

-Spatial Locality: instead of fetching just one item from the main memory to the cache , it is useful to fetch several items that reside at adjacent addresses as well.

5. Define Control store.

-the micro routines for all instructions in the instruction set of a computer are stored in a special memory called control store.

PART-B

II Answer *any five* of the following. Each question carries six marks.

1 State the use of Assembler Directives. Write any five Assembler Directives with their syntax and meaning.

Assembler Directive is a message to the assembler that tells the Assembler something it needs to know in order to carry out the assembly process.

- EQU-which informs the assembler about the value of SUM.

Syntax: SUM EQU 200

- ORIGIN- Tells the assembler program where in the memory to place the data block that follows.

Syntax: SUM ORIGIN 204

- DATAWORD-to inform the assembler of the requirement.

Syntax: N DATAWORD 100

- END-tells the assembler that this is the end of the source program text.

Syntax: END START

- RETURN-it identifies the point at which execution of the program should be terminated.

Syntax: RETURN

2.Give a brief description of pipelining and superscalar operation.

The processor need not wait till the execution of instruction one in order to execute instruction two, rather the processor directly starts executing instruction two, while the instruction one is under execution, this is referred to as pipelining.

Execution of several instructions is possible in a given time slot, this activity is referred as super scalar operation.

3.Explain the Hand-shaked protocol for data transfer over the bus.

The hand shake protocol states that the master places the address and command information on the bus. Then it indicates to all devices that it has done so by activating the Master-ready line .this causes all devices on the bus to decode the address. **Diagram(245)**

4.Discuss the data transfer mechanism of the PCI bus.

During a write operation, the processor sends a memory address followed by a sequence of data words, to be written in successive memory locations starting at that address.

-the PCI is designed primarily to support this mode of operation.

-a read or a write operation involving a single word is simply treated as a burst of length one.

-the bus supports three independent address spaces: memory, I/O, and configuration.

5. Write Notes on Flash memory.

-has similar approach to EEPROM.

-read the contents of a single cell,but write the contents of an entire block of cells.

-flash devices has greater density

-higher capacity and low storage cost per bit.

-power consumption of flash memory is very low,making it attractive for use in equipment that is battery-driven

-single flash chips are not sufficiently large,so larger memory modules are implemented using flash cards and flash drives

6. Compare static and dynamic RAM.

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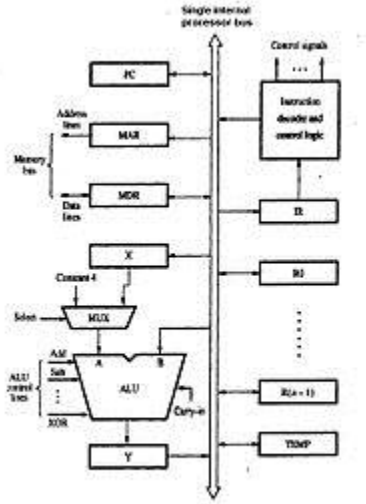
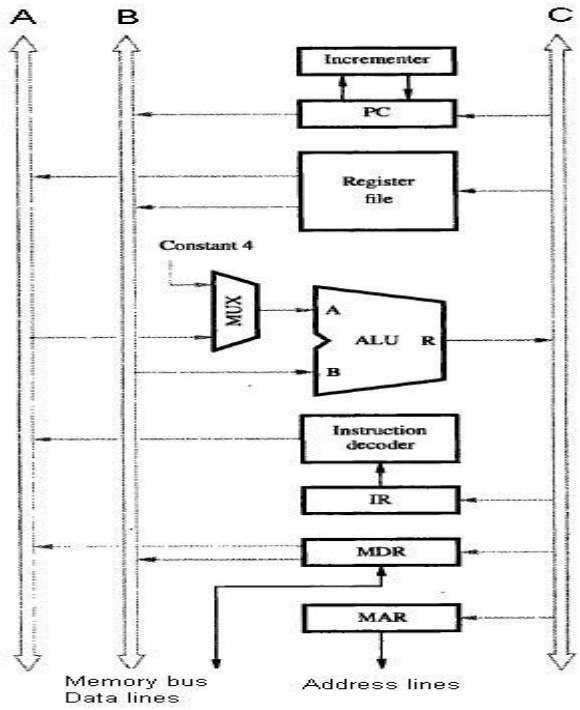
Static RAM	**Dynamic RAM**
It contains less memory less per unit area	It contains more memory cells as compared to static RAM
Less access time hence faster memories	Access time is greater
It consists of number of flip-flops. Each flip-flop stores one bit	It stores the data as a charge on the capacitor. It consists of MOSFET and the capacitor for each cell.
Refreshing circuitry is not required	Refreshing circuitry is required to maintain the change on the capacitors after every few milliseconds. Extra hardware is required to control refreshing. this makes system design complicated.
Cost is more	Cost is less

7.Draw the data path of three bus organization and explain.



Single Bus Organization



Multi Bus Organization

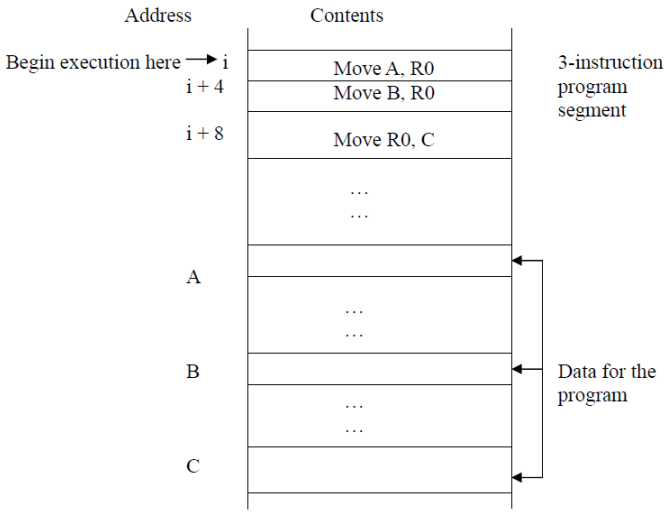
PART—C

(Answer one full question from each unit. Each question carries 15 marks.)

UNIT—I

III Write short notes with necessary diagrams on: **15**

(i) Straight line sequencing.



-one memory operand per instruction
-32-bit word length
-Memory is byte addressable
-full memory address can be directly specify in a single word instruction

To begin executing a program, the address of its first instruction must be placed into the PC.Then the processor control circuit use the information in the PC to fetch and execute instructions,one at a time,in order of increasing addresses,This is called straight line sequencing

During the execution of each instruction the PC incremented by 4 to point to the next instruction

(ii)branching:

	Move N, R1
	Clear R0
LOOP Program loop	Determine address of "Next" number and add "Next" number to R0
	Decrement R1
	Branch >0 LOOP
	Move R0, SUM
	……. ……. …….
SUM	
N	n
NUM1	
NUM2	
	…… …... …...
NUMn	

Fig b Using a loop to add n numbers

To begin executing a program,the address of its first instruction must be placed into the PC.Then the processor control circuit use the information in the PC to fetch and execute instructions one at a time,in order of increasing addresses.

In the case of branch instruction loads a new address into the program counter ,as a result,the processor fetches and executes the instruction at this new address

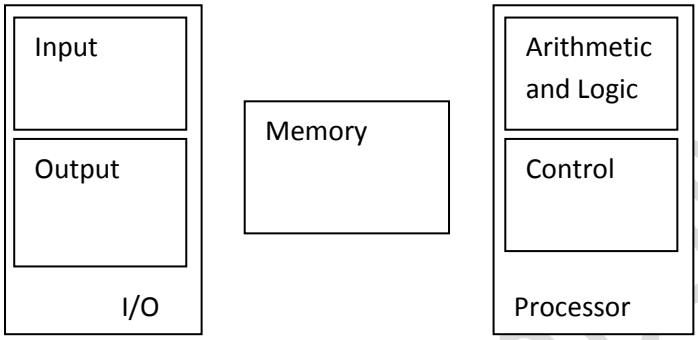
(iii) conditional codes

Conditional code flags/conditional code register/status register

- N(negative):set to 1-if the result is negative;otherwise cleared to 0
- Z(zero):set to 1-if the result is zero;otherwise,cleared to 0
- V(overflow): set to 1-if arithmetic overflow occurs;otherwise cleared to 0
- C(carry): set to 1-if a carry out results from the operation;otherwise,cleared to 0
- Different instructions affect different flags

OR

IV (a) With a neat diagram explain the functional units of a computer. 10



A computer consists of five functionally independent main parts: input, memory, arithmetic and logic, output, and control units

- The input unit accepts the coded information from human operators, from electromechanical devices such as keyboards, or from other computers over digital communication lines.
- This information received is either stored in the computer's memory for later references or immediately used by the arithmetic and logic circuitry to perform the desired operation.
- The results are sent back to the outside world through the output unit
- **Input Unit:**
  - Computers accept coded information through input units, which read the data.
  - EX: Keyboard
    - Whenever a key is pressed,the corresponding letter or digit is automatically translated into its corresponding binary code and transmitted over a cable to either the memory or the processor.
- **Memory Unit:**
  - The function of the memory unit is to store programs and data.
  - There are two classes of storage, called primary and secondary.
  - Programs must reside in the memory during execution.Instruction and data can be written into the memory or read out under the control of the processor
- **Arithmetic and Logic:**
  - Most computer operations are executed in the arithmetic and logic unit(ALU) of the processor.

- EX: consider two numbers located in the memory are added.they are brought in to the processor,and the actual addition is carried out by the ALU.The sum may then be stored in the memory or retained in the processor for immediate use.

- **Output Unit:**
  - Its function is to send Processed results to the outside world
  - EX: Printer, Monitor etc
- **Control Unit:**
  - The control unit is effectively the nerve center that sends control signals to the other units and senses their states.

IV (b) Describe the internal registers of the processor. 5

The Processor contains number of registers used for several different purposes.

Instruction Register (IR): holds the instruction that is currently being executed. its output is available to the control circuits.

Program Counter (PC): It keeps track of the execution of program. It contains the memory address of the next instruction to be fetched and executed.

Memory Address Register (MAR): Holds the address of the location to be accessed.

Memory Data Register (MDR): Contains the data to be written into or read out of the addressed location

n-general purpose registers

UNIT--II

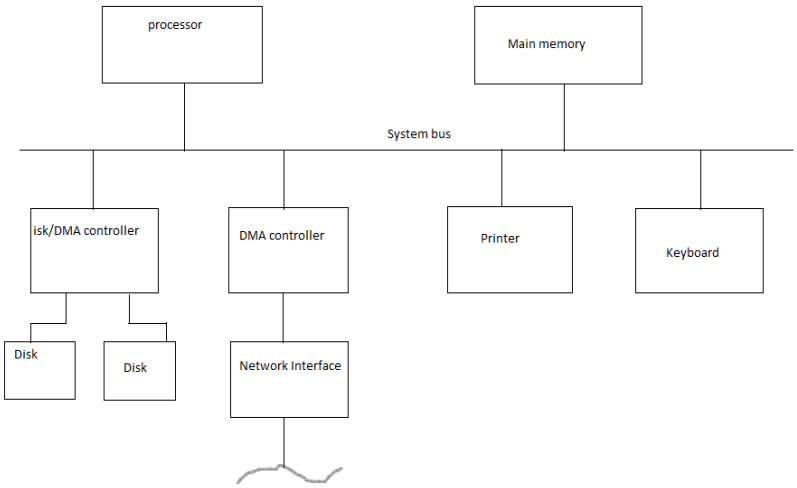
V Explain DMA and illustrate the direct transfer between memory and peripherals. 15

DMA consists of a special control unit which is provided to transfer a block of data directly between an I/O device and the main memory without intervention by the processor.

-when the processor determines that the program that is being executed requires a DMA transfer,it informs the DMA controller which sits in the interface circuit of the device of three things,namely,the starting address of the memory location,the number of words that needs to be transferred,and the direction of transfer that is,whether the data needs to be transferred from the I/O device to the memory or from the memory to the I/O device.

-after initiating the DMA transfer,the processor suspends the program that that initiated the transfer,and continues with the execution of some other program.the program whose execution is suspended is said to be in the blocked state.

-usually,the processor originates most cycles on the bus.the DMA controller can be said to steal memory access cycles on from the bus thus,the processor and the DMA controller use the bus in an interwoven fashion.this interweaving technique is called as cycle stealing



-An alternate approach would be to provide DMA controllers exclusive capability to iniyiate transfers on the bus,and hence exclusive access to the main memory.this is known as the block mode or the burst mode of operation.

- Memory accesses by the processor and the DMA controllers are interwoven.requests by DMA devices for using the bus are always given higher priority than processor requests.
- Among different DMA devices,top priority is given to high speed peripherals such as a disk,a high speed network interface etc.
- The processor originates most memory access cycles,the DMA controller can be said to "steal" memory cycles from the processor.hence this interweaving technique is called *cycle stealing.*
- The DMA controller may be given exclusive access to the main memory to transfer a block of data without interruption.This is known as *block* or *burst* mode.

OR

VI Explain the parallel and serial interfaces. 15

Parallel port:

Parallel ports were originally developed by IBM as a way to connect a printer to the computer.IBM engineers coupled a 25-pin Centronics connector to create a special cable to connect the printer to the computer.

other printer manufactures ended up adopting the centronics interface,making this strange hybrid cable an unlikely de facto standard.

When a PC sends data to a printer or other device using a parallel port,it sends 8 bits of data(1 byte) at a time.

these 8 bits are transmitted parallel to each other,as opposed to the same 8 bits being transmitted serially (all in a single row) through a serial port.

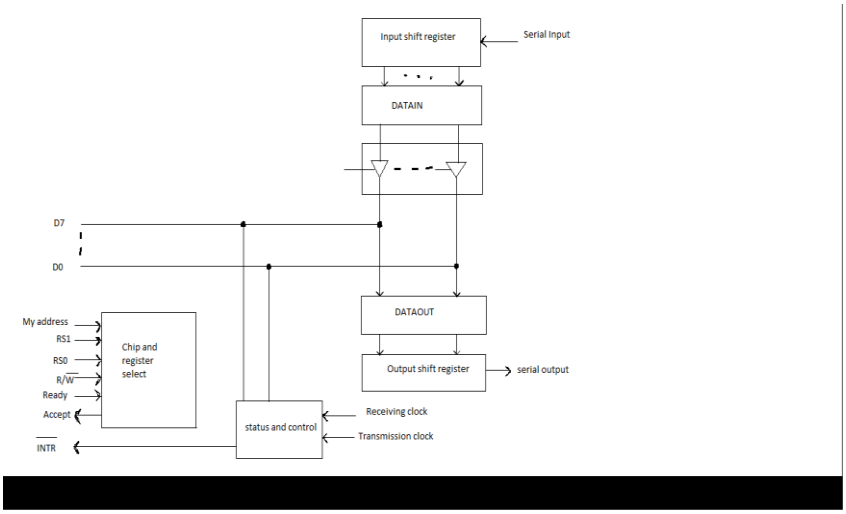
the standard parallel port is capable of sending 50 to 100 kilobytes of data per second

Serial Port:

A serial port is a communication physical interface through which information transfers in or out one bit at a time.

-it is capable of communicating in a bit serial fashion on the device side and in a bit parallel fashion on the bus side.

-the transformation between the parallel and the serial formats is achieved with shift registers that have parallel access capability.



-serial interface

-the part of the interface that deals with the bus is the same as in the parallel interface.

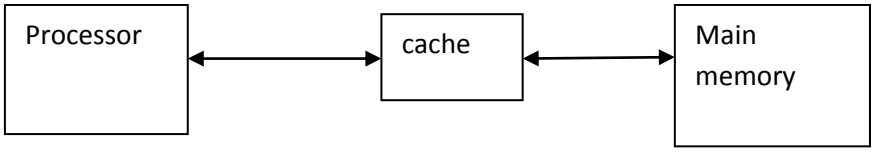
-the double buffering used in the input and output paths is important. a simpler interface could be implemented by turning DATAIN and DATAOUT into shift registers and eliminating the shift registers –

-because serial interfaces play a vital role in connecting I/O devices, several widely used standards have been developed.

UNIT—III

VII (a) Describe the cache memory mechanism **7**

- The CPU of a computer can usually process instructions and data faster than they can be fetched from a reasonably priced main memory unit.
- Using a cache memory, the memory cycle time can be reduced.
- A cache is small, fast memory that is inserted between the larger, slower main memory and the CPU as in.



- Cache is a semiconductor memory. It consists of SRAM's. Its access time is about ions which is less than that of the main memory (50 ns).
- The modern 32-bit and 64-bit microprocessors operate at very high speed.
- There are two types of cache schemes---write through and write back.
- Here both the main memory and cache contains the same data which is a desirable characteristic for direct memory access (DMA).
- This required additional hardwired support, but improves performance, since the exchanges between cache and the main memory are fewer and better timed.
- Cache is placed at two or three levels, called first level(L_1), second level(L_2), third level(L_3).

VII(b) with a neat diagram describe the internal organization of memory chip. 8

each emory cell can hold one bit of information.

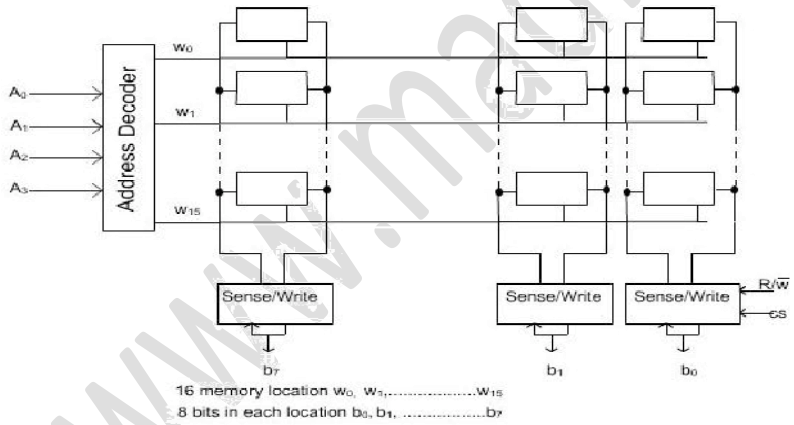
-memory cells are organized in the form of an array.

-one row is one memory word.

-all cells of a row are connected to a common line,known as the "word line".

-word line is connected to the address decoder.

-sense/write circuits are connected to the data input/output lines of the memory chip.



OR

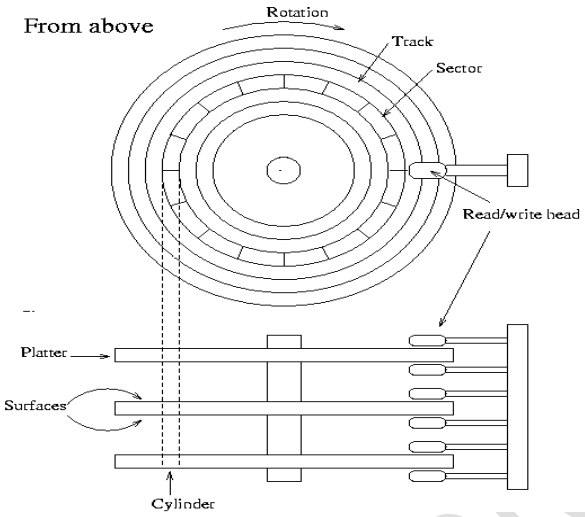
VIII Explain the construction and working of magnetic hard disk. 15

A magnetic hard disk is circular plate constructed of metal or plastic coated with magnetized material. Often both sides of the disk are used and several disks may be stacked on one spindle with read/write heads available on each surface.

All disks rotate together at high speed and are not stopped or started for access purposes.

Bits are stored in the magnetized surface in spots along concentric circles called tracks. the tracks are divided into sectors.

The minimum quantity of information which can be transferred is a sector or group of sectors called clusters.



Here read/write head has to be moved to different tracks for reading and writing. Other units are seperate read/write heads are provided for each track in each surface.

After the read/write heads are positioned in the specified track .Information transfer is very fast once the beginning of a sector has been reached.

A track in a given sector near the circumference is longer than a track near the center of the disk.

To make all the records in a sector of equal length, some disks use a variable recording density with higher density on tracks near the center than on tracks near the circumference.

Disks are permanently attached to the unit assembly and cannot be removed by the occasional user are called *hard disks*

A disk drive with removable disk is called a *floppy disk.*

There are two sizes commonly used magnetic recording materials are:

(i) 5.25” diameter, 1.2 MB capacity/360 KB capacity

(ii) 3.5” diameter, 1.44 MB capacity.

UNIT—IV

IX Explain the steps involved in the execution of instruction MUL R1, (R2), with the control sequences. 15

Consider the instruction,

MUL R1 , (R2)

Which Multiplicate the contents of memory location pointed to by R1.Executing this instruction requires the following actions:

1. Fetch the instruction.
2. Fetch the first operand (the contents of the memory location pointed to by R1).
3. Perform the addition.
4. Load the result into R2.

The sequence of control steps required to perform these operations for the single bus architecture is given below.

1. PC_{out} ,MAR_{in} , Read , Select4 , MUL , Z_{in}
2. Z_{out} , PC_{in} , Y_{in} , WMFC
3. MDR_{out} , IR_{in}
4. $R1_{out}$, MAR_{in} , Read
5. $R2_{out}$, Y_{in} , WMFC
6. MDR_{out} , SelectY , MUL, Z_{in}
7. Z_{out} , $R1_{in}$, End

In step 1:- the instruction fetch operation is initiated by loading the contents of the PC into the MAR and sending a read request to the memory. The select signal is set to Select4,which causes the multiplexer MUX to select the constant4. This value is multiplied to the operand at input B and result is stored in the register Z.

Step 2:-The updated value is moved from register Z back into the PC

Step 3:-The word fetched from the memory is loaded into the IR.

Step 4:-The instruction decoding circuits interprets the contents of the IR and the contents of register R2 are transferred to the MAR and a memory read operation is initiated.

Step 5:- The contents of R2 are transferred to register Y

Step 6:- When a read operation is completed, the memory operand is available in register MDR, and the multiplication operation is performed.

Step 7:-the Product is stored in register Z.

OR

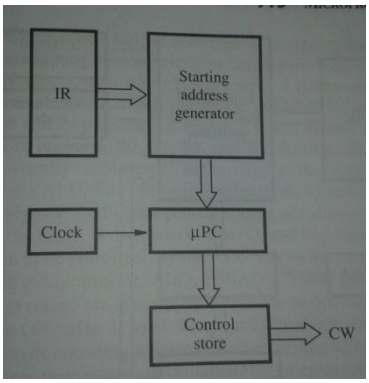
X (a) Discuss the role of cache memory in pipelining. 3

- **E**ach pipeline stage is expected to complete in one clock cycle.
- The clock period should be long enough to let the slowest pipeline stage to complete
- Faster stage can only wait for the slowest one to complete.
- Since main memory is very slow compared to the execution, if each instruction needs to be fetched from main memory, pipeline is almost useless.
- The use of cache memories solves the memory access problem.

(b) with necessary block diagram, explain the organization of microprogrammed control units.12

- Control signals are generated by a program similar to machine language programs.

- When a new instruction is loaded into the IR , the Micro PC is loaded with the starting address of the micro routine for that instruction.
- **Control word(CW);** Is a word whose individual bits represent the various control signals.Each of the control steps in the control sequence of an instruction defines a unique combination of 1s and 0s in the CW
- **Microroutine:** A sequence of CWs corresponding to the control sequence of a machine instruction constitutes the microroutines.
- **Micro instruction:** the individual control words in this microroutine is called micro instruction.



- A straight forward way to structure microinstructions is to assign one bit position to each control signal
- However,this is very inefficient.
- The length can be reduced; most signals are not needed simultaneously,and many signals are mutually exclusive.
- All mutually exclusive signals are placed in the same group in binary coding