TED (10)-3068 Reg. No.....

(REVISION-2010) Signature.....

THIRD SEMESTER DIPLOMA EXAMINATION IN ENGINEERING/ TECHNOLOGY-OCTOBER,2011

COMPUTER ARCHITECTURE

(Common for CM, CT and IF)

[*Time:* 3 hours

(Maximum marks: 100)

Marks

PART –A

I Answer *all* questions in one or two sentences. Each question carries 2 marks

1. Write the need for assembler

Programs written in an assembly language can be automatically translated into a sequence of machine instructions by a program called an assembler.

2. state the function of a bus.

A group of lines that serves as a connecting path for several devices is called a bus.In addition to the lines that carry the data. The bus must have lines for address and control purposes.

3. List the two modes of DMA transfer.

Burst mode (or) block transfer DMA

Cycle steal (or) single byte transfer DMA

4. Give the definition of memory cycle time.

Which the minimum time delay required between the initiation of two successive memory operations

Ex: time delay between two successive read operation

5. Define control word.

Is a word whose individual bits represent the various control signals.Each of the control steps in the control sequence of an instruction defines a unique combination of 1s and 0s in the CW

PART B

II Answer *any five* of the following questions. Each question carries six marks.

UNIT—I

1. Write notes on instruction sequencing

-one memory operand per instruction
-32-bit word length
-Memory is byte addressable
-full memory address can be directly specify in a single word instruction

To begin executing a program, the address of its first instruction must be placed into the PC.Then the processor control circuit use the information in the PC to fetch and execute instructions,one at a time,in order of increasing addresses,This is called straight line sequencing

During the execution of each instruction the PC incremented by 4 to point to the next instruction

2.differentiate between memory maooed I/O and I/O mapped I/O

Memory mapped I/O.

-I/O devices and the memory may share the same address space

-any machine instruction that can access memory can be used to transfer data to or from an I/O device

I/O mapped I/O

-I/O devices and the memory may have different address space

-special instructIons to transfer data to and from I/O devices

-I/O devices may have to deal with fewer address lines

3.illustrate the operation of Universal serial bus.

To accommodate a large number of devices that can be added or remove data any time, the USB has the tree structure as shown in the figure

-Each node of the tree has a device called a hub, which act as an intermediate control point between the host and the I/O devices.

-at the root of the tree, a root hub connects the entire tree to the host computer. the leaves of the tree are the I/O devices being served(for example, keyboard, internet connection, speaker or digital TV).

-in normal operation, a hub copies a message that it receives from its upstream connection to all its downstream ports. As a result, a message sent bythe host computer is broadcast to all I/O devices, but only the addressed device will respond to that message.

However , a message from an I/O device is sent only upstream towards the root of the tree and is not seen by other devices. hence,the USB enables the host to communicate with the I/O devices, but it does not enable these devices to communicate with each other.

4.Discuss the working of magnetic tapes:

The tape is a strip of plastic coated with a magnetic recording medium.bits are recorded as magnetic spots on the tape along several tracks.

7 or 9 bits are recorded simultaneously to form a character together with a parity bit.

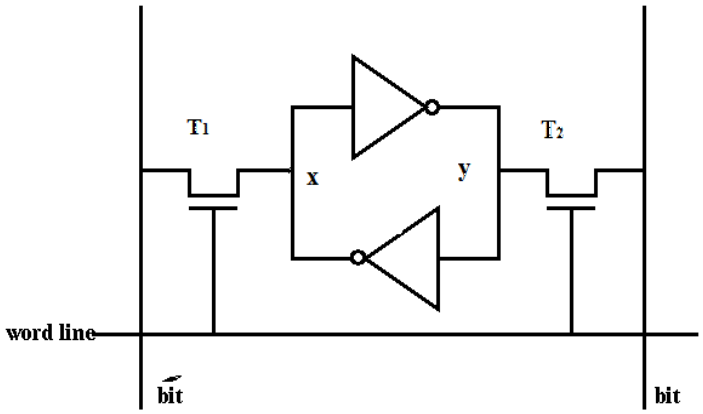
Magnetic tape units can be stopped,started to move forward or in reverse,or can be rewound.

Gaps of unrecorded tape are inserted between records where the tape can be stopped,the tape starts moving while in a gap and attains its constant speed by the time it reaches next record

Each record on tape has an identification bit pattern at the beginning and end.by reading the bit pattern at the beginning, the tape control identifies the record number.

A tape unit is addressed by specifying the record number and the number of characters in the record.records may be of fixed or variable length

5.illustrate the implementation of SRAM.



Two inverters are cross-connected to form a latch.the latch is connected to two bit lines by transistors T1 and T2.These transistors act as switches that can be opened or closed under control of the word line.

When the word line is at ground level, the transistors are turned off and the latch retains its state

Read operation:

In order to read the state of the SRAM cell , the word line is activated to close switches T1 and T2. If the cell is in state 1,the signal on bit line *b* is high and the signal on bit line *b'* is low.

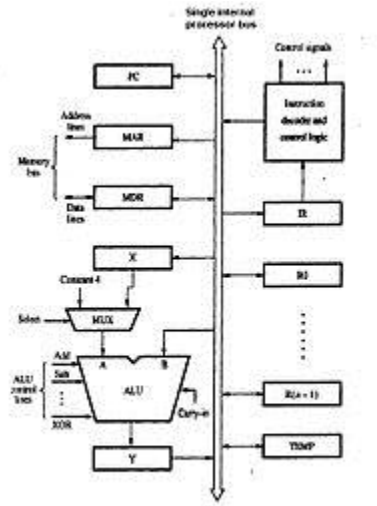
The opposite is true if the cell is in state 0.thus , *b* and *b'* are compliments of each other

Write operation:

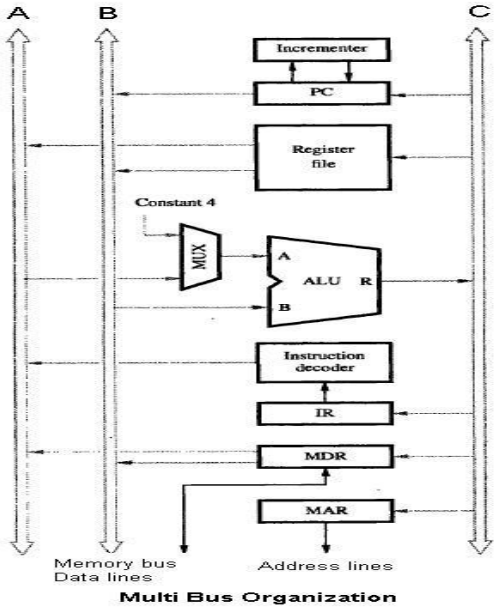
The state of the cell is set by placing the appropriate value on bit line *b* and its compliment on *b'*,and then activating the word line.

6.**Draw the single bus and three bus organization of datapath.**

Single Bus Organization



Three bus organization



7.write the control sequence for branch-on-zero- instruction.

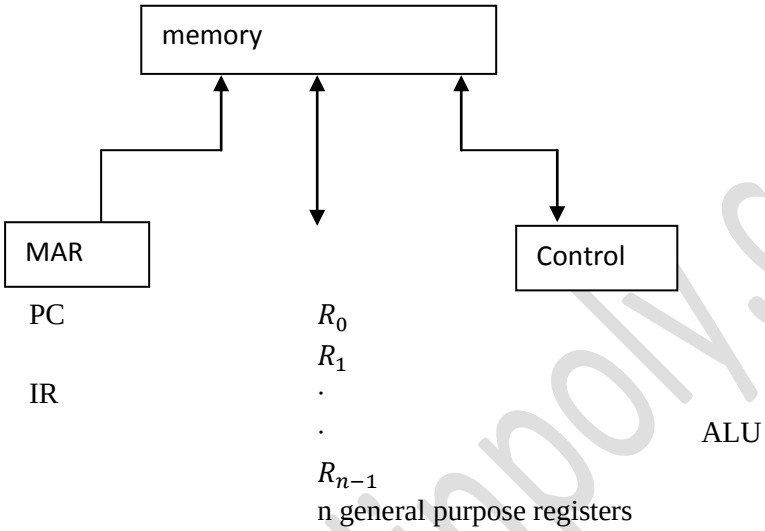
1. PC_{out}, MAR_{in} , Read, Select4, Add, Z_{in}
2. $Z_{out,}$ PC_{in}, Y_{in}, WMFC
3. MDR_{out}, IR_{in}
4. Offset-field-of-IR_{out} , Add , Z_{in}
5. 5.Z_{out} , PC_{in} ,End

PART—C

(Answer one full question from each unit. Each question carries 15 marks.)

UNIT—I

III. With the neat sketch of processor-memory connection, explain the basic operational concepts of a computer system. **15**



registers:

- Instruction register(IR)
- Program counter(PC)
- General-purpose register(R_0-R_{n-1})
- Memory address register(MAR)
- Memory Data register(MDR)

working

- Programs reside in the memory through input devices
- PC is set to point to the first instruction
- the contents of PC are transferred to MAR
- A read signal is sent to the memory
- The first instruction is read out and loaded into MDR
- The contents of MDR are transferred to IR
- Decode and execute the instruction
- Get operands for ALU
    - General-purpose register
    - Memory(address to MAR-read-MDR to ALU)
        - Perform operation in ALU
        - Store the result back
            - To general-purpose register
            - To memory(address to MAR,result to MDR-write)
                - instructionDuring the execution ,PC is incremented to the next instruction

OR

IV.Write short notes on the factors that affect the performance of a computer system. 15

Performance is measured in terms of its accessing capability. hence, performance is nothing but,how fast a computer executes programs.the accessing speed of a computer basically depends on three entities,they are

1.The hardware circuitry through which the computeris made.

2.the design of various instruction sets,supported by a computer.

3.the design of different compilers,which are used in compiling a set of programs.

Processor clock:

In order to organize or schedule the processors activities, a clock is embedded on its circuit board which is referred as processor clock.hence, a given processor performs its activities depending on its clock cycles.

Basic performance equqtion:

$T=\frac{N\times S}{R}$

Where,

T-processor time required to execute a program that has been prepared in high-level language

N-number of actual machine language instructions needed to complete the execution (note:loop)

S-average number of basic stepe needed to execute one machine instruction.Each step completes in one clock cycle

R-clock rate

Pipelining and superscalar operation:

The processor need not wait till the execution of instruction one in order to execute instruction two, rather the processor directly starts executing instruction two, while the instruction one is under execution, this is referred to as pipelining.

Execution of several instructions is possible in a given time slot, this activity is referred as super scalar operation.

Clock rate:

In basic performance equation

$T=\frac{N\times S}{R}$

The quantity 'R' is referred as clock rate which is measured in terms of cycles per second.

CISC and RISC:

Complex Instruction set Computer (CISC) refers to a type of processors which possesses ability to implement certain complex instructions

Reduced Instruction set computer (RISC) refers to another variety of processors which implements a concept such as every instruction is valid to acquire only single word.

Compiler:

A compiler is a program which translates a given high level language program into machine level by passing it through sequence of predefined steps.

Performance measurement:

To measure the performance of the system a new organization was found under the name SPEC or system performance evaluation corporation. this organization framed certain demonstrating program and executed them on different systems.

UNIT--II

V(a).Illustrate the direct data transfer between memory and peripherals. 7

DMA consists of a special control unit which is provided to transfer a block of data directly between an I/O device and the main memory without intervention by the processor.

-when the processor determines that the program that is being executed requires a DMA transfer,it informs the DMA controller which sits in the interface circuit of the device of three things,namely,the starting address of the memory location,the number of words that needs to be transferred,and the direction of transfer that is,whether the data needs to be transferred from the I/O device to the memory or from the memory to the I/O device.

-after initiating the DMA transfer,the processor suspends the program that that initiated the transfer,and continues with the execution of some other program.the program whose execution is suspended is said to be in the blocked state.

-usually,the processor originates most cycles on the bus.the DMA controller can be said to steal memory access cycles on from the bus thus,the processor and the DMA controller use the bus in an interwoven fashion.this interweaving technique is called as cycle stealing

-An alternate approach would be to provide DMA controllers exclusive capability to iniyiate transfers on the bus,and hence exclusive access to the main memory.this is known as the block mode or the burst mode of operation.

V(b).write short notes on: (i) parallel port: 8

Parallel ports were originally developed by IBM as a way to connect a printer to the computer.IBM engineers coupled a 25-pin Centronics connector to create a special cable to connect the printer to the computer.other printer manufactures ended up adopting the centronics interface,making this strange hybrid cable an unlikely de facto standard.

When a PC sends data to a printer or other device using a parallel port,it sends 8 bits of data(1 byte) at a time.these 8 bits are transmitted parallel to each other,as opposed to the same 8 bits

being transmitted serially (all in a single row) through a serial port.the standard parallel port is capable of sending 50 to 100 kilobytes of data per second

(ii). Asynchronous bus:

In asynchronous bus, the common clock is eliminated and data transfer on the system bus is achieved by the use of a handshake between the processor and the device being addressed.here, the clock line is replaced by two control signals ready and accept.

OR

VI (a).Explain the device identification and multiple requests handling method of interrupt driven I/O. 8

-A request is received over the common interrupt request line.additional information is needed to identify the particular device that activated the line.

-It two devices have activated the line at the same time,it must be possible to break the tie and select one of the two requests for service.when an interrupt service routine for the selected device has been completed,the second request can be serviced

The information needed to determine whether a device is requesting an interrupt is available in its status register.when a device raises an interrupt request, it sets to 1 one of the bits in its status register,which will call the IRQ bit

-the simplest way to identify the interrupting device is to have the interrupt service routine poll all the I/O devices connected to the bus.the first device encountered with its IRQ bit set is the device that should be serviced.An appropriate subroutine is called to provide the requested service.

-the polling scheme is easy to implement.its main disadvantage is the time spent interrogating the IRQ bits of all the devices may not be requesting any service.

Vectored Interrupts:

To reduce the time involved in the polling process,a device requesting an interrupt may identify itself directly to the processor.then, the processor can immediately start executing the corresponding interrupt-service routine.

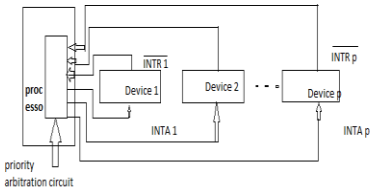
-the term vectored interrupts refers to all interrupt-handling schemes based on this approach.

-a device requesting an interrupt can identify itself by sending a special code to the processor over the bus.this enables the processor to identify individual devices even if they share a single interrupt-request line.

Interrupt nesting:

-Execution of a given interrupt-service routine,once started ,always continues to completion before the processor accepts an interrupt request from a second device.

-interrupt –service routine are typically short,and the delay they may cause in acceptable for most simple devices.



Simultaneous requests:

-the processor must have some means of deciding which request to service first.The processor simply accepts the request having the highest priority.if several devices share once interrupt – request line.

Controlling device requests:

-it is important to ensure that interrupt requests are generated only by those I/O devices that are being used by a given program.Idle devices must not be allowed to generate interrupt requests,even though they may be ready to participate in I/O transfer operations.

VI(b).Describe the sequence of events of data transfer in SCSI . 7

1. The SCSI controller ,acting as an initiator,contents for control of the bus.
2. When the initiator wins the arbitration process,it selects the target controller and hands over control of the bus to it
3. The target starts an output operation (from initiator to target)., in response to this,the initiator sends a command specifying the required read operation
4. The target, realizing that it first needs to perform a disk seek operation , sends a message to the initiator indicating that it will temporarily suspend the connection between them. Then it releases the bus
5. The target controller sends a command to the disk drive to move the read head to the first sector involved in the requested read operation.then, it reads the data stored in the sector an stores them in a data buffer.
6. The target transfers the contents of data buffer to the initiator and then suspends the connection again. data are transferred either 8 or 16 bits in parallel depending on the width of the bus.
7. The target controller sends a command to the disk drive to perform another seek operation.then,it transfers the contents of the second disk sector to the initiator,as before.at the end of this transfer,the logical connection between the two controllers is terminated
8. As the initiator controller receives the data,it stores them into the main memory using the DMA approach.
9. The SCSI controller sends an interrupt to the processor to inform it that the requested operation has been completed.

UNIT—III

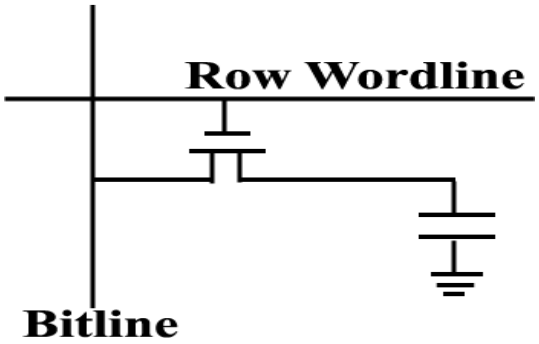
VII(a). Describe Asynchronous and synchronous DRAM. 10

Asynchronous DRAMs:

The timing of the memory device is controlled asynchronously. A specialized memory controller circuit provides the necessary control signals, RAS and CAS,that govern the timing.yhe processor must take into account the delay in the response of the memory.

-such memories are referred to as asynchronous DRAMs.

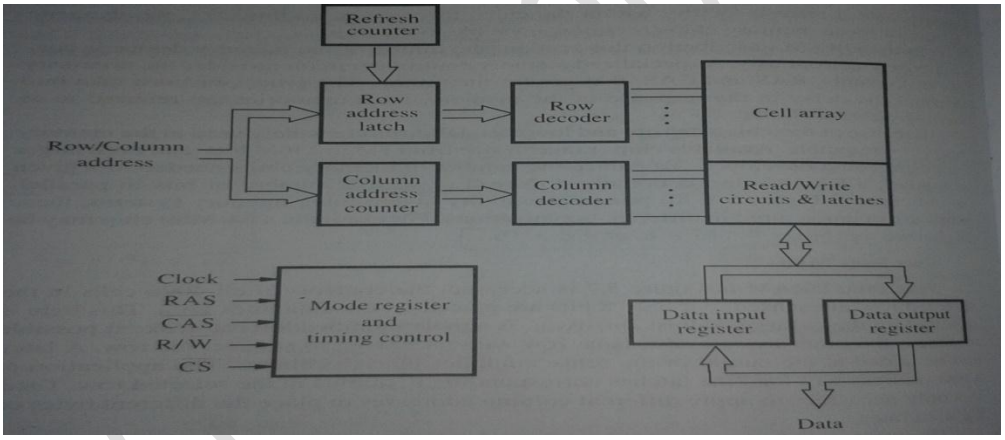
Because of their high density and low cost,DRAMs are widely used in the memory units of computers.



Synchronous DRAMs:

-In DRAMs whose operation is directly synchronized with a clock signal.such memories are known as synchronous DRAMs.

-the address and data connections are buffered by means of registers. SDRAMs have several different modes of operation, which can be selected by writing control information into a mode register



VII(b) write notes on Rambus Memory. 5

-rambus is small company founded in 1989 to develop a new high bandwidth bus, commonly known as rambus

-the reference voltage is about 2V, and the two logic values are represented by 0.3V swings above and below V_{ref} such signalling is known as differential signalling

- rambus provides a complete specification for the design of such communication link, called the rambus channel.

-the rambus allows clock rate of 400MHz and because of data is transmitted on both the edges of the clock,the data transfer rate is 800MHz.

-the circuitry needed to interface DRAM chip to tha rambus channel is also included on the chip.such DRAM chip is known as rambus DRAM or simply RDRAM.

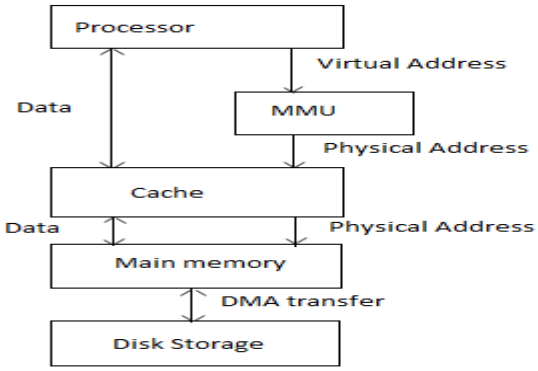
-the rambus DRAM units are connected to the rambus channel.

OR

VIII(a) With a neat sketch,explain the organization of virtual memory. 10

- - Virtual memory is an architectural solution to increase the effective size of the memory system
- Physical main memory in a computer is generally not as large is the entire possible addressable space.
  - Physical memory typically ranges from a few hundred megabytes to 1 G bytes.

- Techniques that automatically move program and data between main memory and secondary storage when they are required for execution are called virtual memory techniques.
- Programs and processors reference an instruction or data independent of the size of the main memory
- Processor issues binary addresses for instructions and data.
  - These binary addresses are called logical or virtual addresses
- Virtual addresses are translated into physical addresses by a combination of hardware and software subsystems.
  - If virtual addresses refers to a part of the program that is currently in the main memory,it is accessed immediately.
  - If the address refers to a part of the program that is not currently in the main memory,it is first transferred to the main memory before it can be used.



- Memory management unit (MMU) translates virtual addresses into physical addresses.
- If the desired data or instructions are in the main memory they are fetched
- If the desired data or instructions are not in main memory, they must be transferred from secondary storage to the main memory.
- MMU causes the operating system to bring the data from the secondary storage into the main memory.

VIII(b) Discuss the different types of ROM's. 5

-**Masked ROM:** In this memory , a bit information is permanently recorded by the masking and metalization process.

It is an expensive an specialized process , but economical for large production quantities

-**PROM(programmable read only memory):**

-this memory is a programmable.

-ROM can be programmed by the user with a special PROM programme that selectively burns the fuses according to the bit pattern to be stored.

-this process is known as “burning the PROM”.

-**EPROM(Erasable Programmable Read Only Memory):**

-It is an erasable PROM.

-Its contents can be erased and can be reprogrammed more than once.

EEPROM(Electrically Erasable PROM):

-it is functionally similar to EPROM,except that information can be altered by using electrical signals at the register level rather than erasing all the information.

Flash Memory:

-it is electrically erasable and programmable.

-the memory chip can be erased and reprogrammed at least a million times.

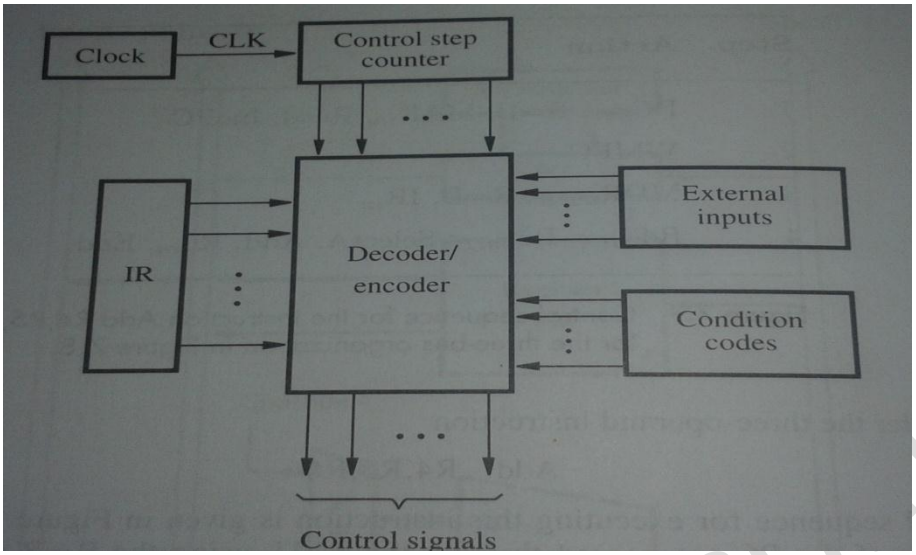
UNIT--IV

IX(a). With necessary diagrams, explain the organization of hardwired control unit 8

-The hardwired control state machine operates at a faster clock rate.

-the control logic is implemented with gates, flip-flops, decoders and other digital circuits.

--it can be optimized to produce a fast mode of operation by having changes in the wiring among the various components.



-Advantages of hardwired control unit:

-the hardwired control unit works fast.

-the combinational circuits generate the control signals based on the input signals status.

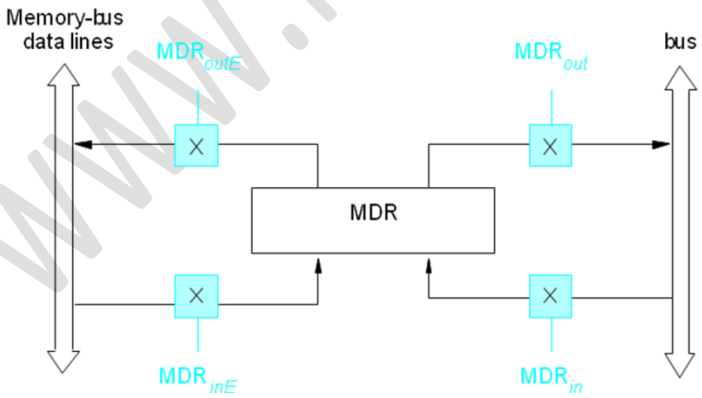
-the delay between the output generation to input availability depends on the number of gates in the path and propagation delay of each gate in the path.

-Disadvantages:

-if the cpu has a large number of control points, the control unit design becomes very complex

-the design does not give any flexibility. if any modification is required, it is extremely difficult to make the correction.

IX(b). Illustrate the connection of MDR with memory bus and system bus **4**



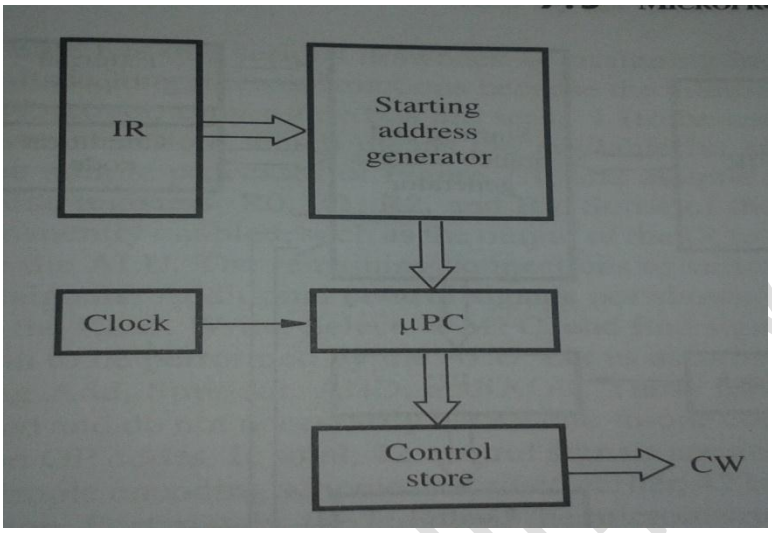
- It has four control signals: MDR_{in} and MDR_{out} control the connection to the internal bus,and $MDR_{in\ E}$ and $MDR_{out\ E}$ control the connection to the external bus
- A three-input multiplexer can be used, with the memory bus data line connected to the third input.this input is selected when $MDR_{in\ E} = 1$.
- A second tri-state gate,controlled by $MDR_{out\ E}$ can be used to connect the output of the flip-flop to the memory bus.

IX(c).write the control sequence for storing a word from register R2 to memory location pointed by R1. **3**

1. $R1_{out}$, MAR_{in}
2. $R2_{out}$, MDR_{in} , Write
3. $MDR_{out\ E}$,WMFC

OR

X(a) Explain micro programmed control unit.List the advantages and disadvantages. **9**



-Each instructon of the processor being controlled causes a sequence of micro instructions called micro program, to be fetched from a special ROM or RAM called a control memory.

-the micro instructions specify the sequence of micro operations or register transfer operations needed to interpret and execute the main instruction.

-Each instruction is fetched from main memory and it indicates a sequence of micro instructions fetching from control memory.

Advantages:

1. The design of microprogram control unit is less complex as compared to the hardwired control unit.
2. The micro program is flexible since modification is easy as it involves simply changing the contents of control memory.
3. A given CPU's instruction set can be easily modified by changing the micro programs without affecting the datapath.
4. The debugging and maintenance of a microprogrammed CPU is easy.

Disadvantages:

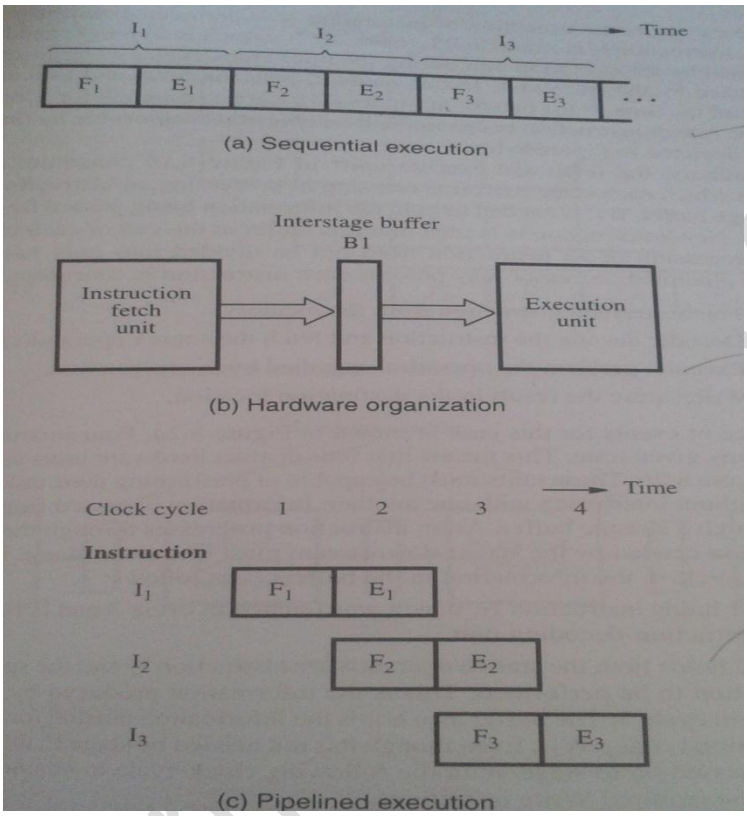
1. A micro programmed CU is slow. The micro instructions are stored in the control memory fetching them takes time.
2. A microprogram CU is expensive as compared to a hardwired CU.

X(a) Discuss the basic concepts of pipelining. **6**

Pipelining is a particularly effective way of organizing concurrent activity in a computer system.

The basic idea is very simple.

-the processor executes a program by fetching and executing instructions, one after the other.



-let F1 and E1 refer to the fetch and executes steps for instruction I1

-execution of a program consists of a sequence of fetch and execute steps