TED (10)-3068 Reg. No.....

(REVISION-2010) Signature.....

THIRD SEMESTER DIPLOMA EXAMINATION IN ENGINEERING/ TECHNOLOGY-MARCH, 2012

COMPUTER ARCHITECTURE

(Common for CM, CT and IF)

[*Time:* 3 hours

(Maximum marks: 100)

Marks

PART –A

I Answer *all* questions in one or two sentences. Each question carries 2 marks

1 Expand CISC and RISC.

CISC-complex instruction set register.

RISC-reduced instruction set register.

2 write the functions of ALU.

It responsible for performing many arithmetic and logic related operations. Ex: addition, subtraction, division, multiplication.

3 Define Interrupt Service Routines.

-Processor is executing the instruction located at address i when an interrupt occurs

-routine executed in response to an interrupt request is called the interrupt service routine

-when an interrupt occurs,control must be transferred to the interrupt service routine

-but before transferring control,the current

Contents of the PC(i+1),must be saved in a known location.

4 define locality of reference

Many instructions in localized areas of the program are executed repeatedly during some period, and the remainder of the program is accessed relatively infrequently. this is referred to as locality of reference

5 write the control sequence for storing the value from a register to main memory

1. $R1_{out}$, MAR_{in}
2. $R2_{out}$, MDR_{in} , Write
3. $MDR_{out\ E}$,WMFC

PART B

II Answer *any five* of the following questions. Each question carries six marks.

1. Write notes on: (i) Multiprocessors

-execute a number of different application tasks in parallel
-Execute subtasks of a single large task in parallel
- All processors have access to all of the memory-shared-memory multiprocessors
-cost-processors, memory units, complex interconnection networks

(ii) Multicomputer:

-Each computer only have access to its own memory
-exchange message via a communication network-message-passing multicomputer

2 Explain the steps involved in assembling and execution of a program.

(i) the assembler assigns addresses to instructions and data blocks
(ii)assembly process determining the values that replace the names
(iii) it keeps tracks of all names and the numerical values the correspond to them in a symbol table.
(iv)the assembler stores the object program on a magnetic disk
Object program proceeds to completion unless there are logical errors in the program.
(v) the assembler can detect and report syntax errors.

3 differentiate between memory mapped I/O and peripheral mapped I/O.

Memory mapped I/O.

-I/O devices and the memory may share the same address space
-any machine instruction that can access memory can be used to transfer data to or from an I/O device

I/O mapped I/O

-I/O devices and the memory may have different address space
-special instructIons to transfer data to and from I/O devices
-I/O devices may have to deal with fewer address lines

4 write the characteristics of : (i) Synchronous bus:

-All devices derive timing information from a common clock signal
-the clock pulse width should be chosen such that it is greater than the maximum propagation delay between the processor and any of the devices connected to the bus.

(ii) Asynchronous bus:

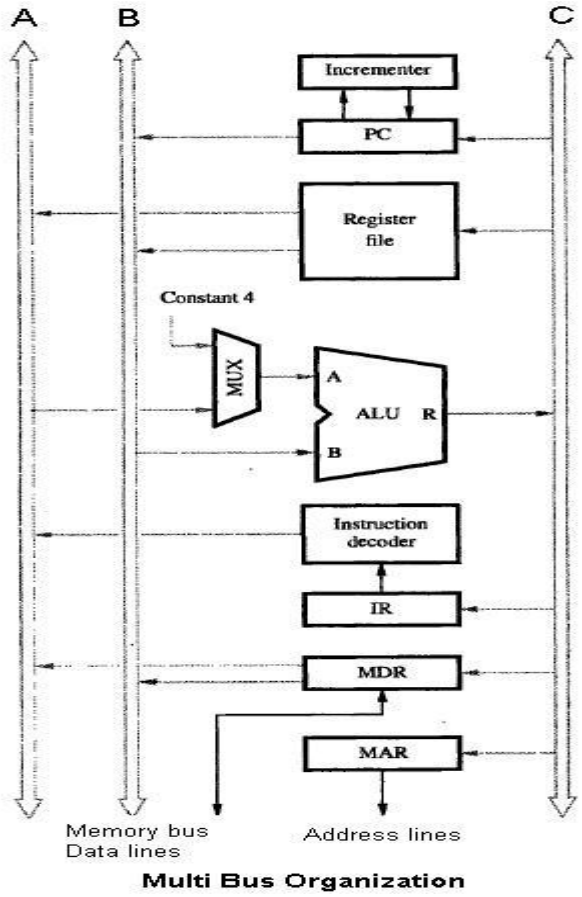
-the common clock is eliminated and data transfer on the system bus is achieved by the use of a handshake between the processor and the device being addressed.

-The clock line is replaced by two control signals ready and accept.

5. Explain the working of magnetic tape systems.

The tape is a strip of plastic coated with a magnetic recording medium.bits are recorded as magnetic spots on the tape along several tracks.
7 or 9 bits are recorded simultaneously to form a character together with a parity bit.
Magnetic tape units can be stopped,started to move forward or in reverse,or can be rewound.
Gaps of unrecorded tape are inserted between records where the tape can be stopped,the tape starts moving while in a gap and attains its constant speed by the time it reaches next record
Each record on tape has an identification bit pattern at the beginning and end.by reading the bit pattern at the beginning, the tape control identifies the record number.
A tape unit is addressed by specifying the record number and the number of characters in the record.records may be of fixed or variable length

6. Draw the architecture of three bus organization



Multi Bus Organization

7. Write the advantages and disadvantages of micro programmed control unit.

Advantages:

-less complex as compared to the hardwired control unit.
-modification is easy.
-the debugging and maintenance of a microprogrammed CPU is easy.

Disadvantages:

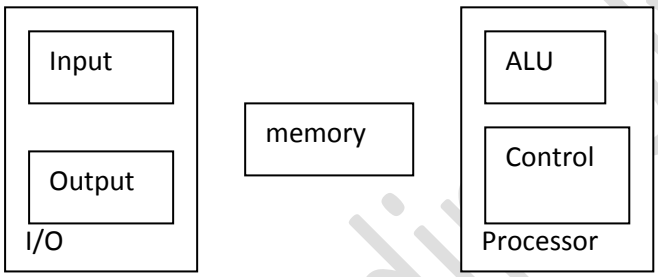
-Is slow
-A microprogram CU is expensive as compared to a hardwired CU
-Design duration is more for a small CPU $(5\times 6 = 30)$

PART—C

(Answer one full question from each unit. Each question carries 15 marks.)

UNIT—I

III With a neat diagram explain the functional units of a computer system. 15



A computer consists of five functionally independent main parts: input, memory, arithmetic and logic, output, and control units

- The input unit accepts the coded information from human operators, from electromechanical devices such as keyboards, or from other computers over digital communication lines.
- This information received is either stored in the computer's memory for later references or immediately used by the arithmetic and logic circuitry to perform the desired operation.
- The results are sent back to the outside world through the output unit
- **Input Unit:**
  - Computers accept coded information through input units, which read the data.
  - EX: Keyboard
    - Whenever a key is pressed,the corresponding letter or digit is automatically translated into its corresponding binary code and transmitted over a cable to either the memory or the processor.
- **Memory Unit:**
  - The function of the memory unit is to store programs and data.
  - There are two classes of storage, called primary and secondary.
  - Programs must reside in the memory during execution.Instruction and data can be written into the memory or read out under the control of the processor
- **Arithmetic and Logic:**

- Most computer operations are executed in the arithmetic and logic unit(ALU) of the processor.
- EX: consider two numbers located in the memory are added.they are brought in to the processor,and the actual addition is carried out by the ALU.The sum may then be stored in the memory or retained in the processor for immediate use.

- **Output Unit:**
  - Its function is to send Processed results to the outside world
  - EX: Printer, Monitor etc
- **Control Unit:**
  - The control unit is effectively the nerve center that sends control signals to the other units and senses their states.

OR

IV Explain the following : **(**$3\times 5 = 15$)

(i) Basic Instruction types

The operation of adding two numbers is a fundamental capability in any computer. The statement

C = A + B

When a program containing this statement is compiled, the three variables, A, B, C are assigned to distinct locations in the memory.The contents of these locations represent the values of the three variables. Hence the above high-level language statement requires the action

C ← [A] + [B]

This three address instruction can be represented symbolically as

Add A,B,C

A general instruction of this type has the format

Operation source1,source2,destination

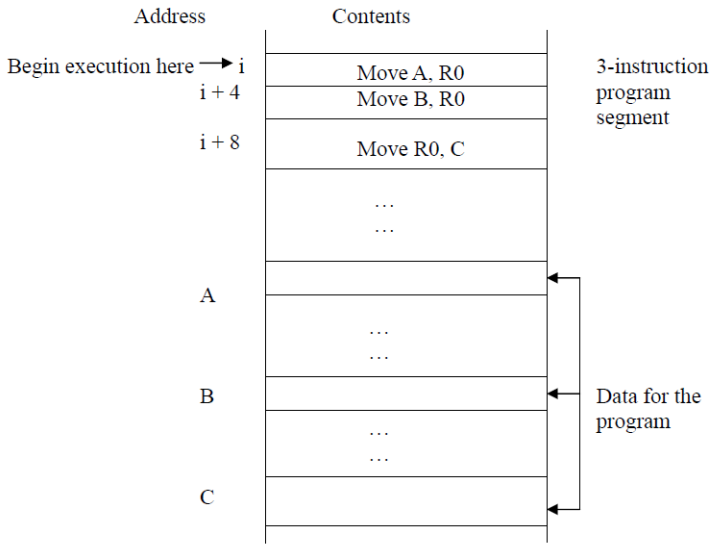
Two address instruction: *Operation source,destination*

An Add instruction: Add A,B

A move instruction: Move A,B

(ii) Straight line sequencing

-one memory operand per instruction
-32-bit word length
-Memory is byte addressable
-full memory address can be directly specify in a single word instruction



To begin executing a program, the address of its first instruction must be placed into the PC.Then the processor control circuit use the information in the PC to fetch and execute instructions,one at a time, in order of increasing addresses, This is called straight line sequencing

During the execution of each instruction the PC incremented by 4 to point to the next instruction

(iii)branching:

	Move N, R1
	Clear R0
LOOP Program loop	Determine address of "Next" number and add "Next" number to R0
	Decrement R1
	Branch >0 LOOP
	Move R0, SUM
	....
SUM	
N	n
NUM1	
NUM2	
	....
NUMn	

Fig b Using a loop to add n numbers

To begin executing a program,the address of its first instruction must be placed into the PC.Then the processor control circuit use the information in the PC to fetch and execute instructions one at a time,in order of increasing addresses.

In the case of branch instruction loads a new address into the program counter ,as a result,the processor fetches and executes the instruction at this new address

UNIT—II

V Explain the parallel and serial interfacing circuits. **15**

Parallel ports: were originally developed by IBM as a way to connect a printer to the computer.IBM engineers coupled a 25-pin Centronics connector to create a special cable to connect the printer to the computer.other printer manufactures ended up adopting the centronics interface,making this strange hybrid cable an unlikely de facto standard.

When a PC sends data to a printer or other device using a parallel port,it sends 8 bits of data(1 byte) at a time.these 8 bits are transmitted parallel to each other,as opposed to the same 8 bits being transmitted serially (all in a single row) through a serial port.the standard parallel port is capable of sending 50 to 100 kilobytes of data per second

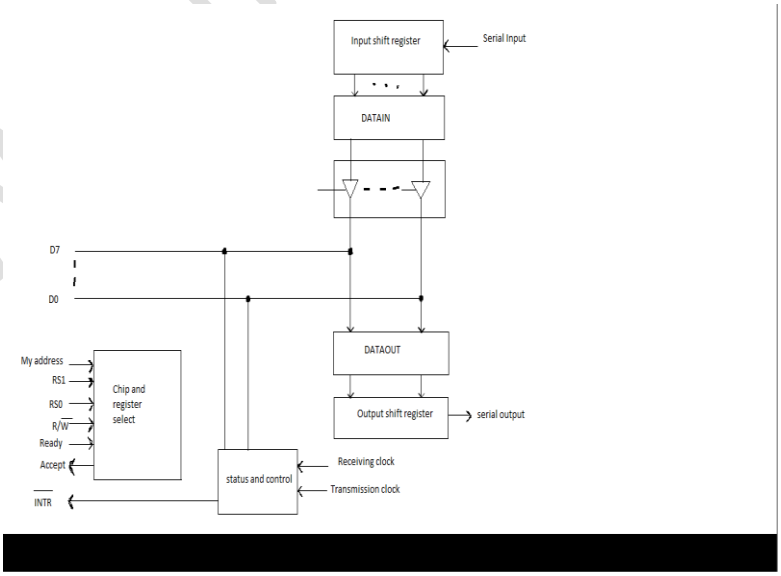
Diagram

Serial Port:

A serial port is a communication physical interface through which information transfers in or out one bit at a time.

-it is capable of communicating in a bit serial fashion on the device side and in a bit parallel fashion on the bus side.

-the transformation between the parallel and the serial formats is achieved with shift registers that have parallel access capability.



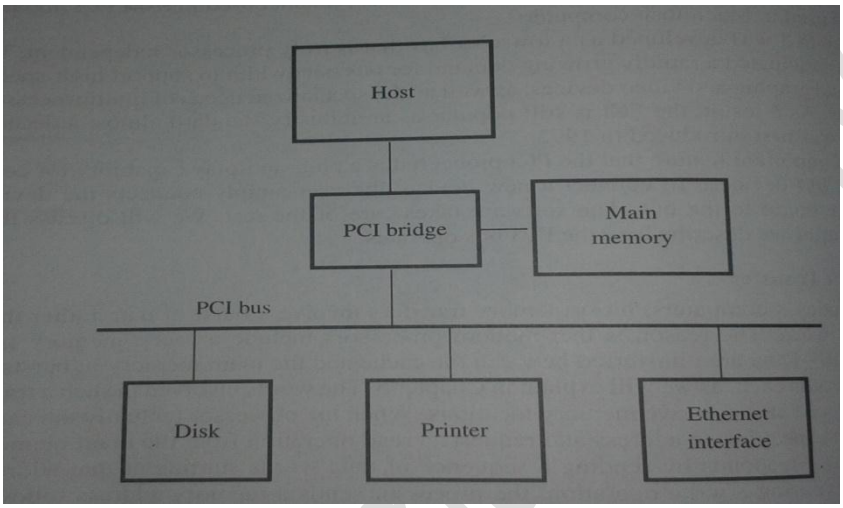
-the part of the interface that deals with the bus is the same as in the parallel interface.

-the double buffering used in the input and output paths is important. a simpler interface could be implemented by turning DATAIN and DATAOUT into shift registers and eliminating the shift registers –
-because serial interfaces play a vital role in connecting I/O devices, several widely used standards have been developed.

OR

VI Write notes on: (i) PCI $(3\times 5 = 15)$

During a write operation, the processor sends a memory address followed by a sequence of data words, to be written in successive memory locations starting at that address.
-the PCI is designed primarily to support this mode of operation.
-a read or a write operation involving a single word is simply treated as a burst of length one.
-the bus supports three independent address spaces: memory, I/O, and configuration.

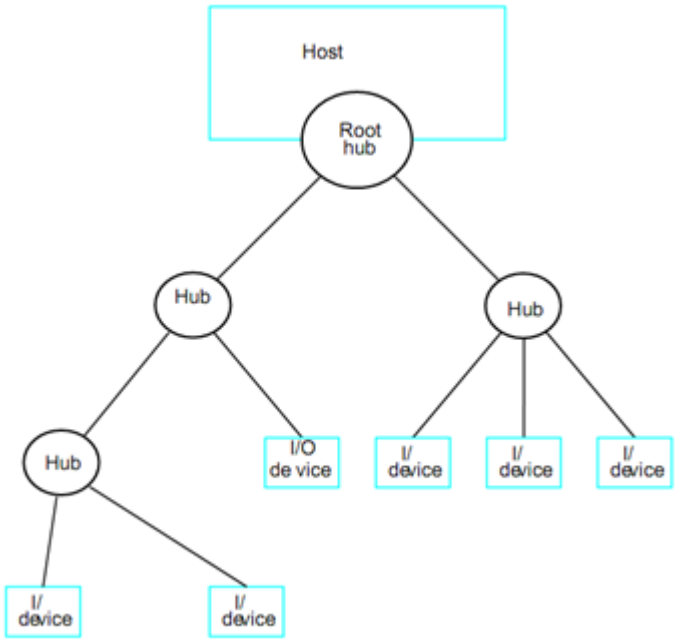


(ii) SCSI

1. The SCSI controller ,acting as an initiator,contents for control of the bus.
2. When the initiator wins the arbitration process,it selects the target controller and hands over control of the bus to it
3. The target starts an output operation (from initiator to target)., in response to this,the initiator sends a command specifying the required read operation
4. The target, realizing that it first needs to perform a disk seek operation , sends a message to the initiator indicating that it will temporarily suspend the connection between them. Then it releases the bus
5. The target controller sends a command to the disk drive to move the read head to the first sector involved in the requested read operation.then, it reads the data stored in the sector an stores them in a data buffer.
6. The target transfers the contents of data buffer to the initiator and then suspends the connection again. data are transferred either 8 or 16 bits in parallel depending on the width of the bus.
7. The target controller sends a command to the disk drive to perform another seek operation.then,it transfers the contents of the second disk sector to the initiator,as before.at the end of this transfer,the logical connection between the two controllers is terminated

8. As the initiator controller receives the data,it stores them into the main memory using the DMA approach.
9. The SCSI controller sends an interrupt to the processor to inform it that the requested operation has been completed.

(iii) USB



-speed

- Low-speed(1.5 Mb/s)
- Full-speed(12 Mb/s)
- High-speed(480 Mb/s)

-port limitation

-Device characteristics

-plug-and-play

-To accommodate a large number of devices that can be added or remove data any time, the USB has the tree structure as shown in the figure

-Each node of the tree has a device called a hub, which act as an intermediate control point between the host and the I/O devices.

-at the root of the tree, a root hub connects the entire tree to the host computer. the leaves of the tree are the I/O devices being served(for example, keyboard, internet connection, speaker or digital TV).

-in normal operation, a hub copies a message that it receives from its upstream connection to all its downstream ports. As a result, a message sent bythe host computer is broadcast to all I/O devices, but only the addressed device will respond to that message.

However , a message from an I/O device is sent only upstream towards the root of the tree and is not seen by other devices. hence,the USB enables the host to communicate with the I/O devices, but it does not enable these devices to communicate with each other.

UNIT--III

VII With a diagram , explain the structure of connecting many memory chips to form a large memory **15**

each emory cell can hold one bit of information.

-memory cells are organized in the form of an array.

-one row is one memory word.

-all cells of a row are connected to a common line,known as the “word line”.

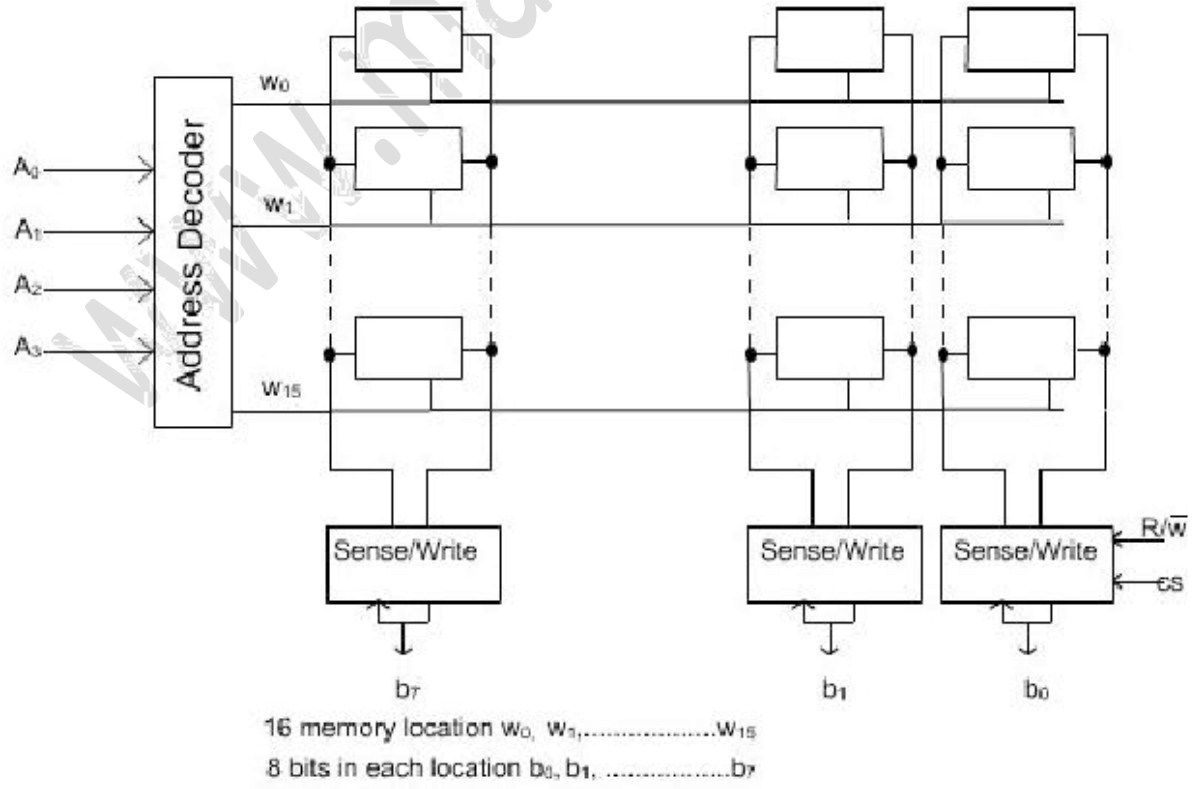
-word line is connected to the address decoder.

-sense/write circuits are connected to the data input/output lines of the memory chip.

Commercially available memory chips contain a much larger number of memory cells than the above.

-Large chips have essentially the same organization , but use a larger memory cell array and have more external connections.
- For example: a 4M-bit chip may have a 512K x 8 organization. In which case 19 address and 8 data input/output pins are needed.now available

- chips with a capacity of hundreds of megabits are



OR

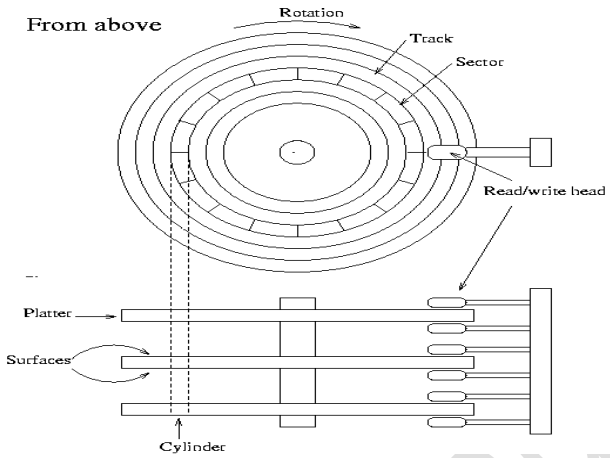
VIII (a) Explain the working of magnetic hard disks with a diagram. 8

A magnetic hard disk is circular plate constructed of metal or plastic coated with magnetized material. Often both sides of the disk are used and several disks may be stacked on one spindle with read/write heads available on each surface.

All disks rotate together at high speed and are not stopped or started for access purposes.

Bits are stored in the magnetized surface in spots along concentric circles called tracks. the tracks are divided into sectors.

The minimum quantity of information which can be transferred is a sector or group of sectors called clusters.



Here read/write head has to be moved to different tracks for reading and writing. Other units are seperate read/write heads are provided for each track in each surface.

After the read/write heads are positioned in the specified track .Information transfer is very fast once the beginning of a sector has been reached.

A track in a given sector near the circumference is longer than a track near the center of the disk.

To make all the records in a sector of equal length, some disks use a variable recording density with higher density on tracks near the center than on tracks near the circumference.

Disks are permanently attached to the unit assembly and cannot be removed by the occasional user are called *hard disks*

A disk drive with removable disk is called a *floppy disk.*

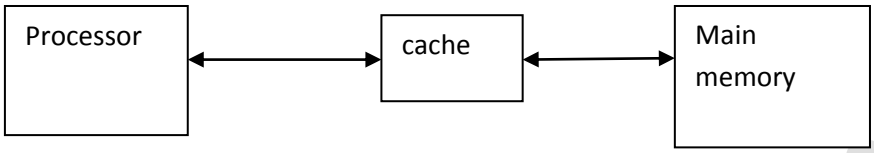
There are two sizes commonly used magnetic recording materials are:

(i) 5.25” diameter, 1.2 MB capacity/360 KB capacity

(ii) 3.5” diameter, 1.44 MB capacity.

VIII (b) Describe the cache memory mechanism **7**

- The CPU of a computer can usually process instructions and data faster than they can be fetched from a reasonably priced main memory unit.
- Using a cache memory, the memory cycle time can be reduced.
- A cache is small, fast memory that is inserted between the larger, slower main memory and the CPU as in.



- Cache is a semiconductor memory. It consists of SRAM's. Its access time is about ions which is less than that of the main memory (50 ns).
- The modern 32-bit and 64-bit microprocessors operate at very high speed.
- There are two types of cache schemes---write through and write back.
- Here both the main memory and cache contains the same data which is a desirable characteristic for direct memory access (DMA).
- This required additional hardwired support, but improves performance, since the exchanges between cache and the main memory are fewer and better timed.
- Cache is placed at two or three levels, called first level(L_1), second level(L_2), third level(L_3).

UNIT--IV

IX Explain the steps involved in the execution of instruction ADD (R1), (R2), with the control sequences. **15**

Consider the instruction,

Add (R1) , (R2)

Which adds the contents of memory location pointed to by R1.Executing this instruction requires the following actions:

1. Fetch the instruction.
2. Fetch the first operand (the contents of the memory location pointed to by R1).
3. Perform the addition.
4. Load the result into R2.

The sequence of control steps required to perform these operations for the single bus architecture is given below.

1. PC_{out} ,MAR_{in} , Read , Select4 , Add , Z_{in}
2. Z_{out} , PC_{in} , Y_{in} , WMFC
3. MDR_{out} , IR_{in}
4. $R1_{out}$, MAR_{in} , Read
5. $R2_{out}$, Y_{in} , WMFC
6. MDR_{out} , SelectY , Add, Z_{in}
7. Z_{out} , $R1_{in}$, End

In step 1:- the instruction fetch operation is initiated by loading the contents of the PC into the MAR and sending a read request to the memory. The select signal is set to Select4,which causes the multiplexer MUX to select the constant4. This value is added to the operand at input B and result is stored in the register Z.

Step 2:-The updated value is moved from register Z back into the PC

Step 3:-The word fetched from the memory is loaded into the IR.

Step 4:-The instruction decoding circuits interprets the contents of the IR and the contents of register R3 are transferred to the MAR and a memory read operation is initiated.

Step 5:- The contents of R2 are transferred to register Y

Step 6:- When a read operation is completed, the memory operand is available in register MDR, and the addition operation is performed.

Step 7:-the Sum is stored in register Z.

OR

X (a) Explain about Hardwired Control unit **9**

-The hardwired control state machine operates at a faster clock rate.

-the control logic is implemented with gates, flip-flops, decoders and other digital circuits.

--it can be optimized to produce a fast mode of operation by having changes in the wiring among the various components.

Diagram(426)

-**Advantages of hardwired control unit**:

-the hardwired control unit works fast.

-the combinational circuits generate the control signals based on the input signals status.

-the delay between the output generation to input availability depends on the number of gates in the path and propagation delay of each gate in the path.

-**Disadvantages:**

-if the cpu has a large number of control points, the control unit design becomes very complex

-the design does not give any flexibility. if any modification is required, it is extremely difficult to make the correction.

X (b) Explain the role of cache memory in pipelining **6**

- **E**ach pipeline stage is expected to complete in one clock cycle.

- The clock period should be long enough to let the slowest pipeline stage to complete
- Faster stage can only wait for the slowest one to complete.
- Since main memory is very slow compared to the execution, if each instruction needs to be fetched from main memory, pipeline is almost useless.
- The use of cache memories solves the memory access problem.