TED (10)-3068 Reg. No.....

(REVISION-2010) Signature.....

THIRD SEMESTER DIPLOMA EXAMINATION IN ENGINEERING/ TECHNOLOGY-OCTOBER, 2013

COMPUTER ARCHITECTURE

(Common for CM, CT and IF)

[*Time:* 3 hours

(Maximum marks: 100)

Marks

PART –A

I Answer the following questions in one or two sentences. Each question carries 2 marks

1. Specify the name of two input units.

A: joystick, trackballs, mouse and key board etc(any two)

2.write the role of program counter

A:Address of the next instruction to be executed

3.Specify the name of two flags/conditional code.

A: N-negative

Z-Zero

V-overflow

C-carry (any two)

4. Discuss the non-volatile memory

A: retain the contents after the power is turned off. Example: ROM, Secondary storage devices

5. Write the stages of two way pipelining.

A: Fetch and Execute $(5\times 2 = 10)$

PART-B

II Answer *any five* of the following. Each question carries six marks.

1. Discuss the basic performance equation.

A: T =$(N \times S) \div R$

T-processor time required to execute a program that has been prepared in high-level language

N-number of actual machine language instructions needed to complete the execution (note: loop)

S-average number of basic stepe needed to execute one machine instruction. Each step completes in one clock cycle

R-clock rate

2. Explain multiprocessors and multicomputer.

A: **Multiprocessors**

-Execute a number of different application tasks in parallel
-Execute subtasks of a single large task in parallel
-All processors have access to all of the memory-shared-memory multiprocessors
-Cost-processors, memory units, complex interconnection networks

Multicomputer

-Each computer only has access to its own memory
-exchange message via a communication network-message-passing multicomputer

3. Differentiate memory mapped I/O and I/O mapped I/O.

A: **Memory mapped I/O.**

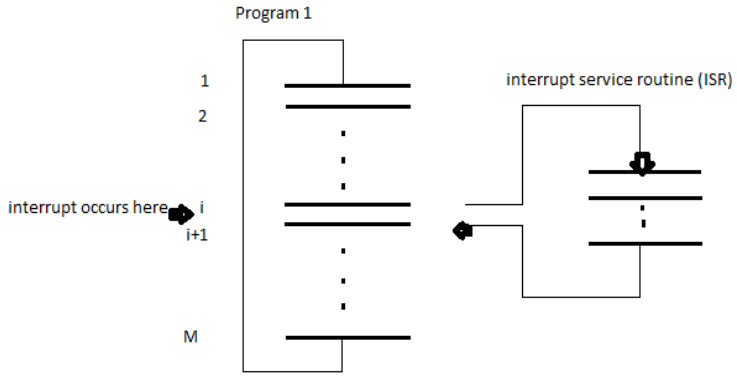
-I/O devices and the memory may share the same address space
-Any machine instruction that can access memory can be used to transfer data to or from an I/O device

I/O mapped I/O

-I/O devices and the memory may have different address space
-special instructions to transfer data to and from I/O devices
-I/O devices may have to deal with fewer address lines

4. Explain the working of interrupt-service routine.

-processor is executing the instruction located at address i when an interrupt occurs-routine executed in response to an interrupt request is called the interrupt service routine
-when an interrupt occurs, control must be transferred to the interrupt service routine
-but before transferring control,the current



Contents of the PC(i+1),must be saved in a known location.
-this will enable the return –from-interrupt to resume execution at i+1.
-return address, or the contents of the PC are usually stored on the processor stack.

5. Write notes on flash memory.

-has similar approach to EEPROM.
-read the contents of a single cell, but write the contents of an entire block of cells.
-flash devices have greater density
-higher capacity and low storage cost per bit.
-power consumption of flash memory is very low, making it attractive for use in equipment that is battery-driven
-single flash chips are not sufficiently large, so larger memory modules are implemented using flash cards and flash drives

6.explain the internal organization of memory chips.

each memory cell can hold one bit of information.
-memory cells are organized in the form of an array.
-One row is one memory word.
-all cells of a row are connected to a common line, known as the "word line".
-word line is connected to the address decoder.
-sense/write circuits are connected to the data input/output lines of the memory chip.

7.Discuss the different steps to execute an instruction. $(5\times 6 = 30)$

-fetch the contents of the memory location pointed to by the PC.the contents of this location are loaded into the IR (fetch phase).

$$IR \leftarrow [\![PC]\!]$$

Assuming that the memory is byte addressable,increment the contents of the PC by 4(fetch phase)

$$PC \leftarrow [PC] + 4$$

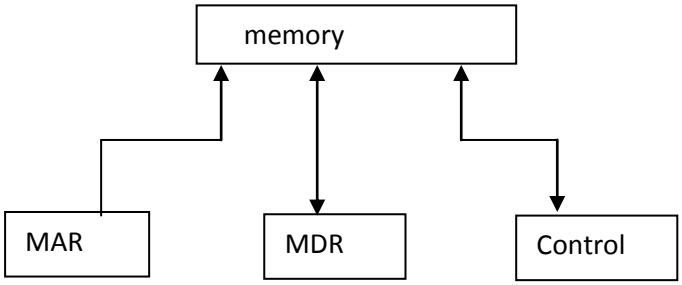
Carry out the actions specified by the instruction in the IR (execution phase)

PART—C

(Answer one full question from each unit. Each question carries 15 marks.)

UNIT--I

III. Explain the basic operational concepts of a computer. 15



PC

IR

R_0
R_1
.
.
R_{n-1}
n general purpose registers

ALU

registers:

- Instruction register(IR)
- Program counter(PC)
- General-purpose register(R_0-R_{n-1})
- Memory address register(MAR)
- Memory Data register(MDR)

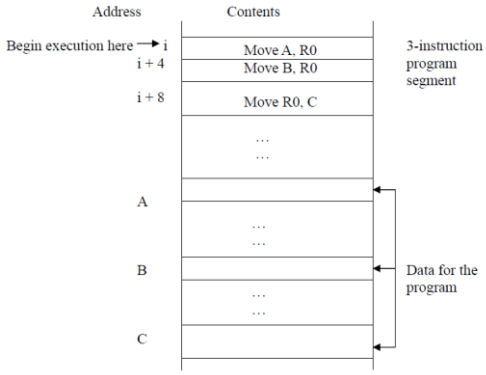
working

- Programs reside in the memory through input devices
- PC is set to point to the first instruction
- the contents of PC are transferred to MAR
- A read signal is sent to the memory
- The first instruction is read out and loaded into MDR
- The contents of MDR are transferred to IR
- Decode and execute the instruction
- Get operands for ALU
  - General-purpose register
  - Memory(address to MAR-read-MDR to ALU)
    - Perform operation in ALU
    - Store the result back
  - To general-purpose register
  - To memory(address to MAR, result to MDR-write)
    - instruction During the execution ,PC is incremented to the next instruction

OR

IV Explain the following: 15

(i) Straight line sequencing



-one memory operand per instruction
-32-bit word length
-Memory is byte addressable
-full memory address can be directly specify in a single word instruction

To begin executing a program, the address of its first instruction must be placed into the PC.Then the processor control circuit use the information in the PC to fetch and execute instructions, one at a time, in order of increasing addresses, This is called straight line sequencing

During the execution of each instruction the PC incremented by 4 to point to the next instruction

(ii)branching:

	Move	N, R1
	Clear	R0
LOOP Program loop	Determine address of "Next" number and add "Next" number to R0	
	Decrement	R1
	Branch >0	LOOP
	Move	R0, SUM
	…… …… …….	
SUM		
N	n	
NUM1		
NUM2		
	…… …… ……	
NUMn		

Fig b Using a loop to add n numbers

To begin executing a program,the address of its first instruction must be placed into the PC.Then the processor control circuit use the information in the PC to fetch and execute instructions one at a time,in order of increasing addresses.

In the case of branch instruction loads a new address into the program counter ,as a result,the processor fetches and executes the instruction at this new address

(iii) Conditional codes

Conditional code flags/conditional code register/status register

- N(negative):set to 1-if the result is negative; otherwise cleared to 0
- Z(zero):set to 1-if the result is zero;otherwise,cleared to 0

- V(overflow): set to 1-if arithmetic overflow occurs; otherwise cleared to 0
- C(carry): set to 1-if a carry out results from the operation;otherwise,cleared to 0
- Different instructions affect different flags

UNIT--II

V (a). Discuss the DMA data transfer **9**

DMA consists of a special control unit which is provided to transfer a block of data directly between an I/O device and the main memory without intervention by the processor.

-when the processor determines that the program that is being executed requires a DMA transfer, it informs the DMA controller which sits in the interface circuit of the device of three things,namely,the starting address of the memory location, the number of words that needs to be transferred, and the direction of transfer that is, whether the data needs to be transferred from the I/O device to the memory or from the memory to the I/O device.

-after initiating the DMA transfer, the processor suspends the program that that initiated the transfer, and continues with the execution of some other program. the program whose execution is suspended is said to be in the blocked state.

-usually, the processor originates most cycles on the bus. the DMA controller can be said to steal memory access cycles on from the bus thus, the processor and the DMA controller use the bus in an interwoven fashion. This interweaving technique is called as cycle stealing

-An alternate approach would be to provide DMA controllers exclusive capability to iniyiate transfers on the bus, and hence exclusive access to the main memory. this is known as the block mode or the burst mode of operation.

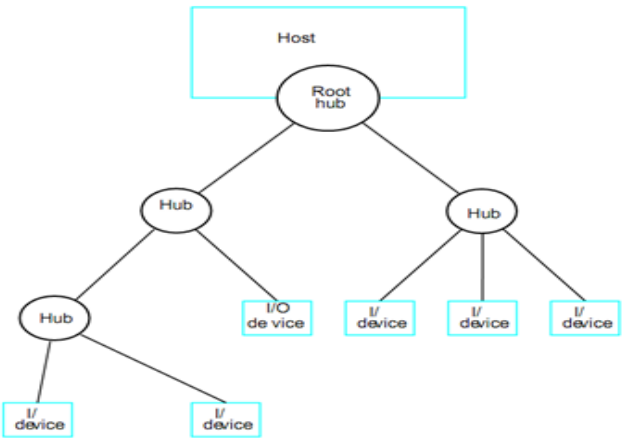
V (b). Explain synchronous bus with timing of input transfer. **6**

Data transfer has to be completed within one clock cycle.

-processor just assumes that the data are available at t2 in case of a read operation, or are read by the device in case of a write operation

OR

VI (a).draw and explain the USB structure. **10**



-speed

- Low-speed(1.5 Mb/s)
- Full-speed(12 Mb/s)
- High-speed(480 Mb/s)

-port limitation

Device characteristics

-plug-and-play

-To accommodate a large number of devices that can be added or remove data any time, the USB has the tree structure as shown in the figure

-Each node of the tree has a device called a hub, which act as an intermediate control point between the host and the I/O devices.

-at the root of the tree, a root hub connects the entire tree to the host computer. the leaves of the tree are the I/O devices being served(for example, keyboard, internet connection, speaker or digital TV).

-in normal operation, a hub copies a message that it receives from its upstream connection to all its downstream ports. As a result, a message sent bythe host computer is broadcast to all I/O devices, but only the addressed device will respond to that message.

However , a message from an I/O device is sent only upstream towards the root of the tree and is not seen by other devices. hence,the USB enables the host to communicate with the I/O devices, but it does not enable these devices to communicate with each other.

VI(b). Explain the polling scheme in interrupt. **5**

If the processor uses a polling mechanism to poll the status registers of I/O devices to determine which device is requesting an interrupt.

In this case the priority is determined by the order in which the devices are polled.

The first device with status bit set to 1is the device whose interrupt request is accepted

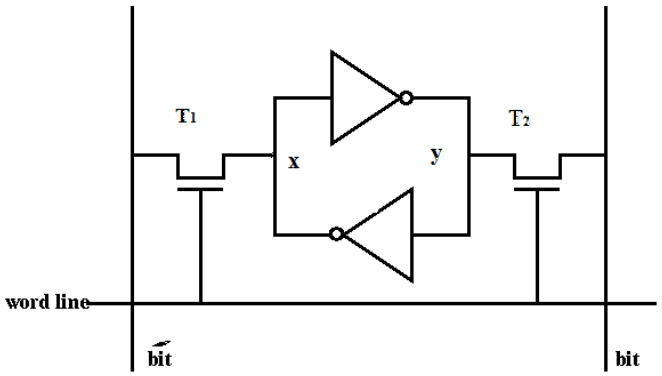
The Polling scheme is easy to implement. Its main disadvantage is the time spent interrogating the IRQ bits of all the devices that may not requesting any service.

UNIT--III

VII(a).Explain SRAM cell **10**

Static RAMs(SRAMs):

- Consist of circuits that are capable of retaining their state as long as the power is applied
- Volatile memories, because their contents are lost when power is interrupted.
- Access times of static RAMs are in the range of few nanoseconds.
- However, the cost is usually high because of several transistors.



- Two transistors inverters are cross connected to implement a basic flip-flop
- The cell is connected to one word line and two bits lines by transistors T1 and T2
- When word line is at ground level, the transistors are turned off and the latch is retains its state
- **Read operation**: in order to read state of SRAM cell, the word line is activated to close switches T1 and T2.sense/write circuits at the bottom monitor the state of b and b'
- **Write operation**: in order to write state of SRAM cell is set by placing value on b and complimented in b' the word line is activated to close switches T1 and T2.this forces cell to corresponding state.

VII(b).Describe memory latency and Memory bandwidth. **5**

Memory latency is the time its takes to transfer a word of data to or from memory

In the case of reading or writing a single word of data, the latency provides a complete indication of memory performance.

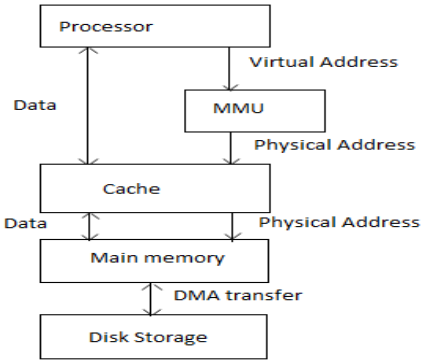
Memory bandwidth is the number of bits or bytes that can be transferred in .The effective bandwidth in a computer system is not determined by solely by the speed of the memory

OR

VIII. Explain the virtual memory and its working **15**

- Virtual memory is an architectural solution to increase the effective size of the memory system

- Physical main memory in a computer is generally not as large is the entire possible addressable space.
    - ♦ Physical memory typically ranges from a few hundred megabytes to 1 G bytes.
- Techniques that automatically move program and data between main memory and secondary storage when they are required for execution are called virtual memory techniques.
- Programs and processors reference an instruction or data independent of the size of the main memory
- Processor issues binary addresses for instructions and data.
    - ▪ These binary addresses are called logical or virtual addresses
- Virtual addresses are translated into physical addresses by a combination of hardware and software subsystems.
    - ♦ If virtual addresses refers to a part of the program that is currently in the main memory, it is accessed immediately.
    - ♦ If the address refers to a part of the program that is not currently in the main memory, it is first transferred to the main memory before it can be used.



- Memory management unit (MMU) translates virtual addresses into physical addresses.
- If the desired data or instructions are in the main memory they are fetched
- If the desired data or instructions are not in main memory, they must be transferred from secondary storage to the main memory.
- MMU causes the operating system to bring the data from the secondary storage into the main memory.

UNIT --IV

IX (a). Explain the complete steps involved in execution of an unconditional branch instruction with the control sequences. 10

- A branch instruction replaces the contents of PC with the branch target address, which is usually obtained by adding an offset X given in the branch instruction.
- The offset X is usually the difference between the branch target address immediately following the branch instruction.

- **Step Action**
    1. PC_{out}, MAR_{in} , Read, Select4, Add, Z_{in}
    2. $Z_{out,}$ PC_{in}, Y_{in}, WMFC
    3. MDR_{out}, IR_{in}
    4. Offset-field-of-IR_{out} , Add , Z_{in}
    5. Z_{out} , PC_{in} ,End

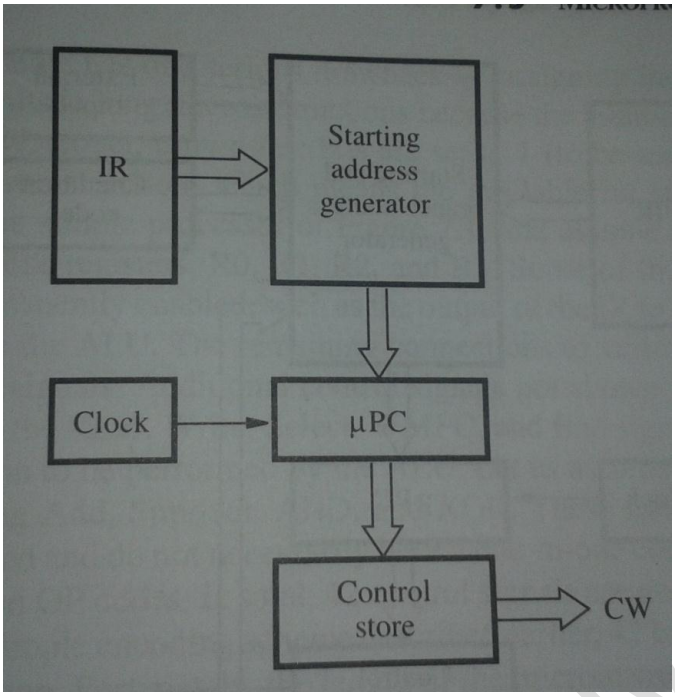
IX(b).Write the role of cache memory in pipelining. **5**

- **E**ach pipeline stage is expected to complete in one clock cycle.
- The clock period should be long enough to let the slowest pipeline stage to complete
- Faster stage can only wait for the slowest one to complete.
- Since main memory is very slow compared to the execution, if each instruction needs to be fetched from main memory, pipeline is almost useless.
- The use of cache memories solves the memory access problem.

OR

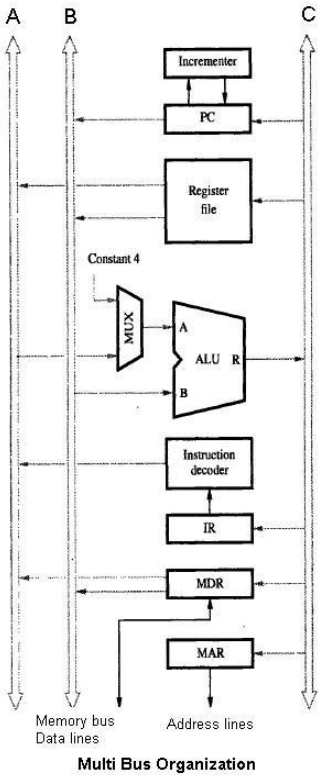
X(a). Explain the micro programmed control unit organization. **10**

- Control signals are generated by a program similar to machine language programs.
- When a new instruction is loaded into the IR , the Micro PC is loaded with the starting address of the micro routine for that instruction.
- **Control word(CW);** Is a word whose individual bits represent the various control signals. Each of the control steps in the control sequence of an instruction defines a unique combination of 1s and 0s in the CW
- **Micro routine:** A sequence of CWs corresponding to the control sequence of a machine instruction constitutes the microroutines.
- **Micro instruction:** The individual control words in this microroutine are called micro instruction.



- A straight forward way to structure microinstructions is to assign one bit position to each control signal
- However, this is very inefficient.
- The length can be reduced; most signals are not needed simultaneously,and many signals are mutually exclusive.
- All mutually exclusive signals are placed in the same group in binary coding

X(b).Draw a multiple-bus organization. **5**



Multi Bus Organization