S3 BE EC

Library

TED (15) – 3042

Reg. No. 15243364

(REVISION — 2015)

Signature

THIRD SEMESTER DIPLOMA EXAMINATION IN ENGINEERING/ TECHNOLOGY — OCTOBER, 2016

DIGITAL ELECTRONICS

(Common to EL, EC and BM)

[*Time* : 3 hours

(Maximum marks : 100)

PART — A

(Maximum marks : 10)

Marks

I Answer the following questions in one or two sentences. Each question carries 2 marks.

1. List different types of number systems.
2. Name the basic logic gates in digital system.
3. State any two advantages of CMOS gates over TTL gates.
4. Write the classifications of sequential circuits.
5. Define modulus of a counter. (5×2=10)

PART — B

(Maximum marks : 30)

II Answer *any five* of the following questions. Each question carries 6 marks.

1. Change the following hexadecimal numbers to equivalent binary.
   (a) 35 (b) 98
   (c) 170 (d) 2469
2. State various scales of integration of digital ICs.
3. List the features of ECL logic family.
4. Explain the working of master - slave JK flip-flop with block diagram.
5. Draw and explain the working of ring counter.
6. Differentiate between synchronous and asynchronous counter.
7. Draw and explain flash type Analog to digital converter(ADC). (5×6=30)

Marks

PART — C

(Maximum marks : 60)

(Answer *one* full question from each unit. Each full question carries 15 marks.)

UNIT — I

III (a) Compute the following binary arithmetic operation using 2's complement method.
(i) 11011-10100 (ii) 10000-11011 8

(b) Implement X-OR gate and X-NOR gate using NAND gates only. 7

OR

IV (a) Change the following expression to reduced form using Boolean laws.

$F = \overline{(A+\overline{BC})}\ (A\overline{B}+ABC)$ 8

(b) Solve the expression, $F = \sum m\ (0, 2, 3, 4, 5, 6)$ using K-Map. 7

UNIT — II

V (a) Draw and explain TTL inverter. 8

(b) Explain the operation of 4 × 1 multiplexer with logic diagram. 7

OR

VI (a) Point out the features of CMOS logic families. 8

(b) Draw and explain half adder using NAND gates only. 7

UNIT — III

VII (a) Draw and explain the working of serial-in serial-out shift register. 8

(b) Explain SR flip-flop using NAND gates with truth-table. 7

OR

VIII (a) Discuss the working of D flip-flop with figure and truth table. 8

(b) Draw and explain serial-in parallel-out shift register. 7

UNIT — IV

IX (a) Implement mod-10 asynchronous counter using JK flip-flop. 8

(b) Explain R-2R ladder type digital to analog converter (DAC). 7

OR

X (a) Draw and explain successive approximation type Analog to Digital Converter. 8

(b) Explain mod-8 synchronous counter with diagram. 7